DAVID A. NESHEIM
1718 BROADWAY
ROCKFORD, ILL. 61108

4-½ DIGIT TRI-PHASIC™ DIGITAL MULTIMETER (Battery or Line Powered)

MODEL 1455

Instruction Manual

MP MASTER
MA28630

DATA PRECISION
... years ahead

ROCKFORD INSTRUMENT LAB
1718 Broadway
Rockford, IL 61108

4-½ DIGIT TRI-PHASIC™ DIGITAL MULTIMETER (Battery or Line Powered)

MODEL 1455

Instruction Manual

DAVID A. NESHEIM
1718 BROADWAY
ROCKFORD, ILL. 61108

DATA PRECISION
... years ahead

COPYRIGHT 1977

DATA PRECISION CORPORATION

PROPRIETARY NOTICE

The information contained in this publication is derived in part from proprietary and patent data of the Data Precision Corporation. This information has been prepared for the express purpose of assisting operating and maintenance personnel in the efficient use of the Model 1455 Digital Multimeter and publication of this information does not convey any rights to reproduce it or to use it for any purpose other than in connection with the installation, operation, and maintenance of the equipment described herein.

CONTENTS

1 INTRODUCTION

1.1 GENERAL
1.2 OPERATING AND DISPLAY FEATURES
1.3 SPECIFICATIONS

2 OPERATION & CALIBRATION

2.1 GENERAL
2.2 UNPACKING
2.3 KEY POINTS ON YOUR MODEL 1455 DMM
2.4 OPERATING PROCEDURES
2.5 CALIBRATION
2.6 APPLICATION NOTES

3 PRINCIPLES OF OPERATION

3.1 INTRODUCTION
3.2 OVERALL BLOCK DIAGRAM
3.3 INPUT SIGNAL CONDITIONING
3.4 TRI–PHASIC A/D CONVERTER (ANALOG PORTION)
3.5 END OF CONVERSION AND POLARITY SENSING
3.6 A/D CONVERTER (DIGITAL SECTION)
3.7 DISPLAY
3.8 ISO-POLAR REFERENCE GENERATION
3.9 DC/DC CONVERTER

4 MAINTENANCE

4.1 GENERAL
4.2 TROUBLE SHOOTING FLOW CHART
4.3 TEST POINTS
4.4 CLOSED–METER TESTS (FIELD MAINTENANCE) TS4-1
4.5 OPEN–METER TEST/MAINTENANCE
4.6 TEST EQUIPMENT
4.7 DC/DC CONVERTER TEST & POWER TS4-2
4.8 REFERENCE VOLTAGE GENERATOR TS4-3
4.9 DIGITAL LOGIC TS 4-4
4.10 A/D CONVERTER & SIGNAL CONDITIONERS TS4-5

5 PARTS LISTS

5.1 MAIN PC BOARD ASSEMBLY
5.2 DC/DC CONVERTER ASSEMBLY
5.3 DISPLAY ASSEMBLY

6 REFERENCE SCHEMATIC

Frontispiece. Model 1455 DMM

Chapter 1

INTRODUCTION

1.1 GENERAL

The Data Precision Model 1455 (frontispiece) is a battery or line-charged battery 4 1/2 digit multimeter for measuring DC or AC voltages, DC or AC currents, or resistances with 0.005% resolution in 21 range scales and with 100% overrange capability. The Model 1455 uses Data Precision's field proven Tri-Phasic™ analog-to digital conversion, Isopolar™ referencing, and Ratiohmic™ resistance measurement designs which provide laboratory-grade performance of high accuracy, stability, and reliability.

The Model 1455 digital multimeter (DMM) is delivered in a complete, ready-to-use configuration, including battery, test probes, and this complete instruction manual of operation and maintenance. The detachable power line cord is included, and the instrument may be switch-controlled in the field to permit use of either 115V or 230V (nominal) source power.

The Model 1455 DMM replaceable, rechargeable battery pack is always being charged when the line cord is attached to the appropriate line power source. A minimum of 6 hours of accurate performance is provided by a fully charged battery. Spare battery packs may be obtained for extended field use where no AC source is available.

1.2 OPERATING AND DISPLAY FEATURES

Model 1455 DMM is operated simply by selecting an appropriate full scale range with one front panel rotary switch and a measurement mode with the other. The measured input signal is displayed on 7-segment planar characters, and the polarity of DC measurements is automatically displayed while the decimal point tracks the manual selection of the full scale range.

Measurements up to 100% overrange beyond the full scale will be within the specified accuracy and displayed as for in-range measurements. Overload signals, beyond the overrange limits on any selected range scale, are automatically sensed, and an Overload indication display is presented. The overload display retains the polarity sign and decimal indication, while blanking all the decimal digits. This is a signal to shift to a higher full scale range. The Model 1455 circuitry is protected against damage from an overload signal within the limits allowed by the specifications.

1.3 SPECIFICATIONS

FUNCTIONAL CHARACTERISTICS

(All modes and ranges)
Reading Rate: 2.5 readings/sec.
Polarity: Autopolarity.
Conversion Technique: Triphasic (see page 4).
Overload Indication: Blanking of all digits, leaving polarity and decimal point illuminated.
Overrange: 100%, except on 1000V ranges as noted.
Common-Mode Rejection Ratios (minimum) with 1000Ω source-impedance unbalance:
120dB at DC. > 100dB at 50 and 60Hz.
Common-Mode Voltage: 500V DC (or peak AC) maximum
Normal-Mode Rejection Ratio: 50dB at 50 and 60Hz.

DC VOLTS

Nominal Range	Overrange	Least-Significant Digit
±1.0000 VDC	±1.9999	100μV
±10.000 VDC	±19.999	1mV
±100.00 VDC	±199.99	10mV
±1000.0 VDC	±1000.0	100mV

Input Impedance:
±1.0000 range, > 1000 Megohms; all other ranges, 10 Megohms.
Maximum Voltage (all ranges): ±1000 Volts.
Resolution: .005%
Accuracy (all ranges, including overrange)

6 months, 23°C ±5°C: ±0.02% rdg ± 0.01% f.s. ± 1 l.s.d.
Add Voltage Coefficient of ±0.00001% (0.1PPM) of rdg/Volt . . . significant only on 1000V range.
Temperature Coefficient (0° C to 40° C, all ranges): (±.003% rdg ±.001% f.s.)/°C.

AC VOLTS

Nominal Range	Overrange	Least-Significant Digit
1.0000 VAC	1.9999	100μV
10.000 VAC	19.999	1mV
100.00 VAC	199.99	10mV
500 VAC	500*	100mV

*See maximum voltage limitation, below.

Input Impedance (all ranges): 1 Megohm in parallel with 50pF or less.
Sensing and Calibration: True Average Sensing, calibrated in RMS of sinewave.
Resolution: .005%
Accuracy (6 months, 23°C ±5°C), all ranges:
at 30Hz: ±0.5% rdg ±.02% f.s.
from 50Hz to 1kHz: ±0.08% rdg ±.02% fs.
at 10kHz: ±0.6% rdg ±.02% f.s.
at 50kHz: ±1.0% rdg ±.05% f.s.
(Linearly interpolate between stated points to calculate accuracy at intermediate frequencies.)
Temperature Coefficient (0°C to 40°C, all ranges):
from 30Hz to 1kHz: (±0.01% rdg ±0.002% f.s.)/°C
at 10kHz: (±0.1% rdg ±0.002% f.s.)/°C
at 50kHz: (± 0.15% rdg± 0.002% f.s.)/°C
(Linearly interpolate between stated points to calculate intermediate temperature coefficients).
Maximum Input Voltage (sinewave RMS):
30Hz to 10kHz: 500V
above 10kHz: decreases linearly to 200V at 50kHz
Settling Time (to settle within ±0.1% of final reading for a full-scale step input): 2.5 sec.

ENVIRONMENT

Temperature Ranges: Operating, 0°C to +40°C
Storage, −25°C to +50°C
Humidity: 80% RH, max

PHYSICAL

The Model 1455 measures only 3½" (8.89cm)H x 8½" (21.59)W x 7¼" (18.415)D without handles, and weighs 3-3/4 lb (1.7025Kg). The handles, which are also used as a tilt stand, increase the overall width to 9 3/4" and add a 2" extension to the depth for carrying, or to the height for stand.

DC CURRENT

Nominal Range	Overrange	Least-Significant Digit
±1.000mA	±1.999mA	1μA
±10.00mA	±19.99mA	10μA
±100.0mA	±199.9mA	100μA
±1000.mA	±1999.mA	1mA

Maximum Current: Series fuse (2A) rated at 32V.
Nominal full-scale voltage drop across shunts: 100mV.
Resolution: .05%
Accuracy (6 months, 23°C ±5°C):
±1.000mA range: ±0.1% rdg ±1 l.s.d.
±10.00mA range: ±0.1% rdg ±1 l.s.d.
±100.0mA range: ±0.2% rdg ±1 l.s.d.
±1000.mA range: ±0.2% rdg ±1 l.s.d.
Temperature Coefficient (0°C to 40°C):
±1.000mA range: (±0.01% rdg ±0.001% f.s.)/°C
±10.00mA range: (±0.01% rdg ±0.001% f.s.)/°C
±100.0mA range: (±0.02% rdg ±0.001% f.s.)/°C
±1000.mA range: (±0.02% rdg ±0.001% f.s.)/°C

AC CURRENT

Nominal Range	Overrange	Least-Significant Digit
1.000mA	1.999mA	1μA
10.00mA	19.99mA	10μA
100.0mA	199.9mA	100μA
1000.mA	1999.mA	1mA

Nominal full-scale voltage drop across shunts: 100mV.
Sensing and Calibration: True-Average Sensing, calibrated in RMS of sinewave.
Resolution: .05%
Accuracy (6 months, 23°C ±5°C), all ranges:
at 30Hz: ±0.7% rdg ±1 l.s.d.
from 50Hz to 1kHz: ±0.3% rdg ±1 l.s.d.
at 10kHz: ±0.7% rdg ±1 l.s.d.
at 50kHz: ±1.8% rdg ±1 l.s.d.
Temperature Coefficient (0°C to 40°C, all ranges):
from 30Hz to 1kHz: (±0.03% rdg ±0.003% f.s.)/°C
at 10kHz: (±0.12% rdg ±0.003% f.s.)/°C
at 50kHz: (±0.17% rdg ±0.003% f.s.)/°C
(Linearily interpolate between stated points to calculate intermediate temperature coefficients).

RESISTANCE

Nominal Range	Overrange	Least-Significant Digit
1.0000kΩ	1.9999kΩ	100mΩ
10.000kΩ	19.999kΩ	1Ω
100.00kΩ	199.99kΩ	10Ω
1000.0kΩ	1999.9kΩ	100Ω
10.000MΩ	19.999MΩ	1000Ω

Maximum Test Current (occurs at zero Resistance-Under-Test):

Range	Current
1kΩ	1.8mA
10kΩ	330μA
100kΩ	35μA
1000kΩ	3.5μA
10MΩ	0.35μA

Configuration: Two-wire
Maximum Open-Circuit Voltage: 3.5 Volts
Resolution: .005%
Accuracy (6 months, 23°C ±1°C):
1kΩ range: ±.07% rdg ±1 l.s.d.
10kΩ range: ±.07% rdg ±1 l.s.d.
100kΩ range: ±.07% rdg ±1 l.s.d.
1000kΩ range: ±0.1% rdg ±1 l.s.d.
10MΩ range: ±0.25% rdg ±1 l.s.d.
Temperature Coefficient (0°C to 40°C):
1kΩ range: (±0.005% rdg ±0.001% f.s.)/°C
10kΩ range: (±0.005% rdg ±0.001% f.s.)/°C
100kΩ range: (±0.005% rdg ±0.001% f.s.)/°C
1000kΩ range: (±0.01% rdg ±0.001% f.s.)/°C
10MΩ range: (±0.02% rdg ±0.005% f.s.)/°C
Settling Time (in seconds): 0.7 + 0.3 x Resistance in Megohms.
Maximum Input Voltage: ±115V DC, or 115 AC (RMS).

POWER SUPPLY

The Model 1455 DMM may be operated from either nominal 115V (105 to 125) or nominal 230V (210-250) line voltage at (47 to 63Hz) or line frequency. An interval manually operated switch adapts the instrument for the selected power source.

The internally mounted battery module (C55P) is rated at 750mA-Hrs at nominal 7.2 volts. It provides a minimum of 6 hours of in-spec performance when fully charged, and requires 12 hours to recharge from a fully discharged condition. The battery is under continuous charge when the line cord is connected to appropriate power source.

Standard equipment furnished with the Model 1455 includes:

1 line cord (double-ended)
1 pair test leads
Operator's manual
Maintenance Manual
Factory-Test Data Sheets
Certificate of Conformance
One-year Warranty

Accessories

High Voltage Probe, Model V-30
Quantity Discounts Available.

Battery module C55P

Chapter 2

OPERATION & CALIBRATION

2.1 GENERAL

The Model 1455 DMM has been shipped with a set of probe leads, and a fully charged battery pack. It is usable immediately upon receipt. The line cord may be connected to the receptacle in the rear panel and to the proper power source, if desired. The battery will be charged at any time the cord is connected to a power source, whether or not the DMM is in use.
This chapter contains:

(1) an inventory list of what you should find upon opening your packing carton;

(2) a complete description of the operating controls and indications;

(3) a step-by-step procedure for operating the instrument in any of its 5 measuring modes;

(4) a step-by-step procedure for recalibrating your meter; and

(5) application notes to help you obtain the measurement accuracies of which your meter is capable

2.2 UNPACKING

The Model 1455 is shipped in a molded protective fitted container. This manual has been packed in a recess at the top of the outer protective layer, and should be read before attempting to use the meter. When the protective box is opened, you should find the following items

(1) Model 1455 4 1/2 Digit Multimeter

(2) Two probes;

(3) One line cord (double-ended)

(4) Certificate of Conformance and Copies of authenticated Factory Test Data Sheets;

(5) Warranty Card;

Carefully examine these articles, noting especially the matching serial numbers of the instrument and the test data. Inspect the packing case and the instrument for any signs of damage during shipment and report immediately to the carrier. Fill out and return the warranty card to register your instrument and to establish your warrantied service interval.

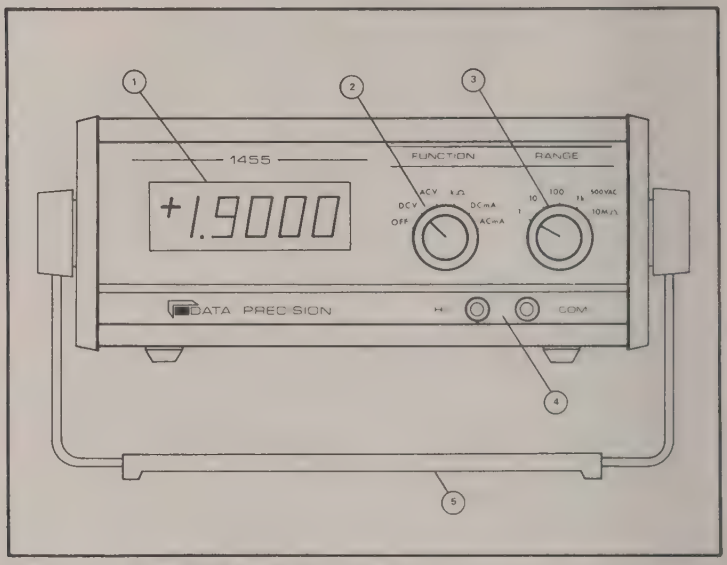


Figure 2-1 Model 1455 DMM, Front Panel

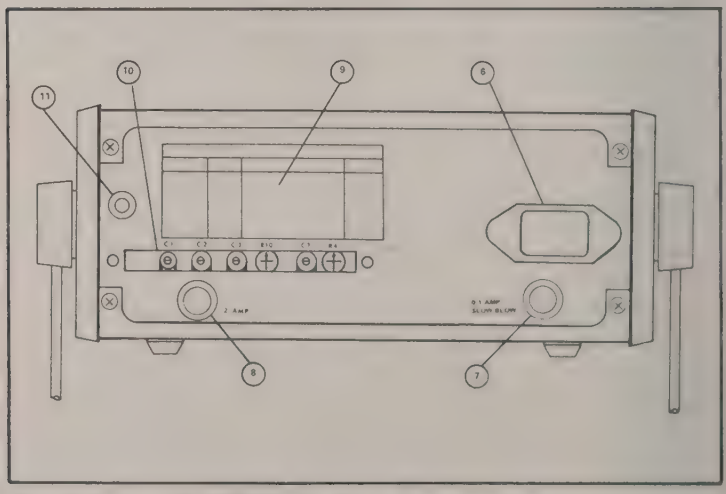


Figure 2-2 Model 1455 DMM, Rear Panel

2.3 KEY POINTS ON YOUR MODEL 1455 DMM (Figures 2-1 and 2-2)

Fig. Item	Name	Description/Function
1	Display	4 Decimal digits and MSD "1"; range-selected decimal point display; automatic polarity (+ and –) indication. 7-segment plasma planar display units.
2	Function	Rotary 6-position switch. Selects one of 5 measuring functions and OFF.
3	Range	Rotary 5-position switch. Selects one of four full-scale ranges for voltage or current measurements, or one of five full-scale ranges for resistance measurements. Decimal point location is located by same selection.
4	Inputs HI and COM	Receptacles for probe terminals. COM designation for reference lead of DC measurements. HI input polarity with respect to COM input is displayed automatically.
5	Handle/Support	Carrying handle; also sued as tilt-up support for bench use.
6	Line cord receptacle	For 110 or 220 VAC inputs. (Source selection switch internally mounted.)
7	Fuse; 1/10 Slow Blow	Power-protect fuse; protects against effects of excessive drain by a malfunctioning instrument.
8	Fuse 2A	Input-protect fuse; protects instrument circuits against excessive current (>2A) inputs. When in DCmA or ACmA functions.
9	Calibration Table	Calibration Instructions Procedural Sequence
10	Adjustments	6 calibrating adjustments for range scales.
11	Test Point	To check battery charge

2.4.1 General

a) If using AC power, be sure the Model 1455 is set up for the correct input line voltage and that a battery pack is mounted in the clips on the rear panel.
b) Turn the instrument ON by selecting the desired measurement function with the Function Mode Switch . . . . DCV, ACV, etc.
c) Select the appropriate full scale range . . . 1K, 100, 10, etc.
d) Connect test leads to meter and apply probes to circuit under test.
e) Read display
f) Select different full scale range value for highest resolution capability.

2.4.2 Applying Power

The Model 1455 4-1/2 digit multimeter may be operated from power supplied by the internal battery module containing six rechargeable NiCd batteries or from the 110VAC or 220VAC power mains if the line cord is connected properly. Before operating, perform a battery charge check as described below. A fully charged battery module will supply up to six hours of in-spec operation, and 12 hours are required to restore a fully discharged battery module to full charge. Note: the batteries are always being charged when the line cord is connected to the power source.

The battery module must always be installed, whether operating from line or not. It provides a required regulating and impedance matching function for the AC/DC converter circuit.

To check the battery charge, use the DMM in DCV function and Range 10. Place the HI probe in the test point on the rear panel (See Figure 2-2). A negative measurement with a value in excess of 7.2 indicates a charged battery.

2.4.3 Selecting Measuring Function

The left-hand, six-position rotary Function Switch turns the meter measuring circuits on, and makes the required internal connections to measure DC volts, AC volts, Kilohms, DC milliamperes, or AC milliamperes. The switch positions are as shown in Table 2-1.

2.4.4 Selecting Full-Scale Range

The right-hand rotary Range Switch selects the full-scale range to be displayed, and simultaneously positions the decimal point for direct reading. The switch positions and the full-scale reading are shown in Table 2-2. Note that the least significant (fifth) digit is blanked for current measurements. Note also that the 10MΩ position is used only for resistance measurements.

2.4.5 Connecting the Inputs

Connect the probes: red probe lead to the HI receptacle and the black probe lead to the COM receptacle of the meter. Measurements made at the sensing ends of the probes will be the value of the HI input with respect to the COM input. If the meter reads +17.724 Volts DC, then the HI (red-lead) terminal is 17.724 Volts higher in potential (more positive) than the COM (black-lead) terminal.

Table 2-1 Function Switch Mode Selection

FUNCTION SWITCH POSITION (clockwise from OFF)	PARAMETER MEASURED (or Instrument Status)
OFF	Disconnects power from battery to meter; Retains charging action to battery if line cord/battery charger are connected.
DCV	DC voltages up to 1,000 volts
ACV	Up to 500 VRMS of true-average-calibrated in RMS AC voltage, from 30Hz to 10KHz, decreasing linearly to 200 V at 50KHz.
KΩ	Resistance in kilohms up to 1000 kilohms, and in megohms up to 20 megohms, with maximum open circuit voltage of 3.5 volts, and able to withstand connected external voltage of ±115V DC or 115V AC RMS. Can be >115V in higher ranges.
DCmA	Direct Current in milliamperes, up to 2,000mA, protected by 2-ampere fuse rated at 32V in red imput probe.
ACmA	Alternating Current in milliamperes. Up to 2,000mA of true average value calibrated in RMS of equivalent sinewaves.

Table 2-2 Range Switch FSR Selection

Switch Position Marking (Clockwise from top)	Nominal Full Scale	Overrange	Units		
			Voltage	Current	Resistance
1.0	.9999	1.9999	V	mA	KΩ
10	9.999	19.999	V	mA	KΩ
100	99.99	199.99	V	mA	KΩ
1K	999.9	(Note 1)	V	mA	KΩ
10MΩ	9.999	19.999	–	–	MΩ

*Least significant digit blanked on current readings; and additional 100% overrange possible.

(Note 1): See specification para 1.3 for overrange limits on these scales.

2.4.6 Reading the Display

DC polarities are automatically indicated on the display, and reflect the polarity of the HI signal with respect to the COM. AC measurements are indicated with a positive polarity sign.

Overrange values up to 100% above the selected full scale range will be measured and displayed. The maximum indication is 19999 with the appropriate decimal point location (and a blanked right hand digit on current measurements).

Overrange measurements of more than 100% above the selected full scale range are indicated by a blanking of all digits, leaving only the polarity of overload and decimal point display lighted. For example, if the applied signal is more than +19.999 volts on the 10 volt full scale range, only the + sign and the decimal point will appear.

2.5 CALIBRATION

2.5.1 General

The Model 1455 Digital Multimeter is factory calibrated and burned-in prior to shipment, and is designed to remain in calibration for a minimum of 6 months before recalibration procedure should be required. The complete set of factory test data sheets for each instrument are shipped with the meter.

2.5.2 Test Instrumentation and Preparation

When recalibration is required, test standards of the following range and accuracy should be used:

DC Volts:		0 to	1.0000V ± 0.01%
AC Volts:	at 100 Hz:	0 to	1.0000V ± 0.05%
	at 20 KHz:	0 to	1.000. V ± 0.10%

Calibrating adjustments are accessible through the rear panel behind the removable cover in the lower left hand side of the rear panel. (See Figure 2-1.) Circuit designation for each adjustment control is shown in Figure 2-2.

NO ZERO ADJUSTMENT IS EVER REQUIRED ON ANY MEASUREMENT FUNCTION OR RANGE SCALE AND NONE IS PROVIDED.

2.5.3 Calibration Procedures

Perform the adjustments in the sequence listed below. Apply test inputs of an amplitude and frequency as close as possible to those listed. Adjust the designated control until the display indicates the exact value of the test input applied. If the only test standard available does not provide the full scale values shown in the table below, then the closest value to the specified input should be used, and the control adjusted for that display value. It is desirable to use input signals of at least 50% of full scale if that option is available.

Table 2.3 Calibration Adjustments

Function Select	FSR Range Select	Test Signal	Adjustment Marking
DCV	1.0	+ 1.9000 VDC	R10
ACV	1.0	100 Hz, 1.9000 V RMS	R4
ACV	1000	20 KHz. 200.00 V RMS	C7
ACV	100	20 KHz, 100.00 V RMS	C3
ACV	10	20 KHz, 19.000 VRMS	C2
ACV	1.0	20 KHz, 1.9000 VRMS	C1

Adjust until the display indicates the value of the test input.

WARNING

Use insulated calibration tool.
High voltage may be present at calibration points.

Note that calibration of other function modes is implicit in the adjustments made according to the table above. This results because the circuit design utilizes the same attenuation networks in common among the different signal conditioning functions.

2.6 APPLICATION NOTES

2.6.1 General

Optimum performance is obtained from your Model 1455 by observing a number of precautions in establishing the test measurement conditions. The few hints included in this paragraph are only indicative of the types of measuring environment problems which may influence the meter performance. It is suggested that the user add his own application aids in the space provided.

2.6.2 Avoiding Ground Loops (Making Grounded Measurements)

If, when the line cord is connected, a potential difference may exist between the "ground" of the power source and the "ground" of the measured circuit. This difference of ground potentials may set up ground-loop currents and affect the measured values although the instrument will reduce their effects significantly (CMRR = 120dB, NMR =50dB).

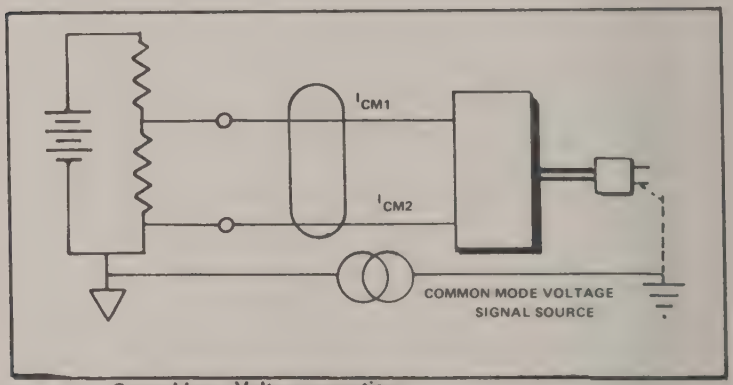


Figure 2-3. **Ground Loop Voltage generation**

2.6.3 Making "Floating" Measurements

In a floating measurement, such as in Figure 2-4, it is possible to introduce a common mode voltage by reactive coupling through the AC power line when that source of Model 1455 power is connected.

2.6.4. Making High Resistance Measurements

When making measurements of very high impedance sources, as when required to measure resistance on the 10 MΩ full scale range, the input circuit is extremely susceptible to noise. The effect of voltage-producing noise fields on the probe leads may be sufficient to introduce significant changes in the least significant digit of the display.

Measurement errors may be kept to a minimum under these circumstances by keeping the leads as short as possible (do not use any extensions on the probes), and by twisting the probe leads so as to equalize any field effects on the signal input leads.

NOTE: **It is good practice to twist probe leads whenever possible in order to equalize any field effects on the signal input leads.**

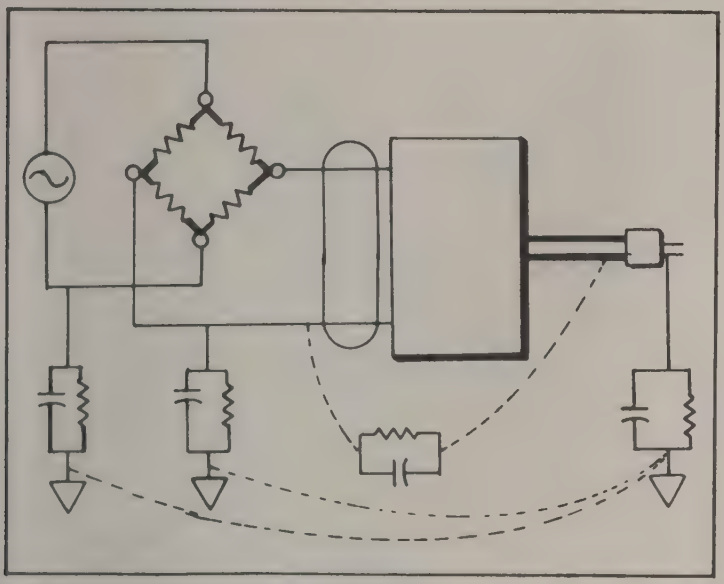


Figure 2-4. Induced AC common mode voltages

2.6.5 Making Very Low Voltage Measurements.

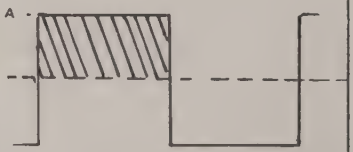
Problems may arise when measuring very low voltages because of the differences in temperature of the probe contact points. Both probes are plated brass, and if the HI probe is in contact with copper in a high ambient temperature, for example, in a computer tape drive mechanism, while the COM probe is grounded at a very much cooler steel cabinet frame, then a difference in emf of several hundred microvolts may result, changing the least significant digit. In order to minimize such errors, connect the probes wherever possible at approximately the same temperature.

2.6.6 Making Complex Waveform AC Measurements

The Model 1455 is calibrated in equivalent RMS values of a sine wave whose average value is the value actually measured by the multimeter, Thus, if a non-sinusoidal waveform is applied at the input the displayed value may be in error, depending upon the extent of the difference in waveforms.

The Model 1455 develops a DC voltage from an AC input by half-wave rectification and the ratio of RMS to average halfwave of a sine wave is 2.2:1. The corresponding ratios for other sample waveforms are included in Figure 2-5.

Table 2-4. Multiplying Factors for Non-Sinusoidal Waveform Measurements

WAVEFORM	AVG VALUE PER MODEL 1450	RMS VALUE	MULTIPLY DISPLAY BY
	.707A	.707A	1.0
	1.11A	1A	0.903
	.555A	.574A	1.034

Chapter 3

PRINCIPLES OF OPERATION

3.1 INTRODUCTION

Model 1455 DMM is triggered automatically to initiate the 3-phase measurement cycle. During phase 1 the meter circuits are automatically servoed to determine the correction for the accumulated zero offsets in the analog integrator loop. In phase 2 the signal to be measured, which has been conditioned according to the type of signal (AC, DC, Ohms) and selected range scale (X1, X10, . . . X1000), is connected in series with the zero offset correction to the dual slope A/D converter integrator which integrates the conditioned input for a fixed time interval of 100 milliseconds. After the fixed time interval of phase 2, phase 3 begins in which the input signal is disconnected from the A/D converter, and in its place a reference signal of opposite polarity and fixed magnitude, is connected in series with the zero offset correction. The integration of the reference signal continues in phase 3 until this second ramp of the dual ramp A/D converter reduces the charge on the integrating capacitor to zero. The zero level on the integrating capacitor is sensed, and it indicates the End of Conversion (EOC) if it occurs in 200 msec or less during phase 3. If there has not been an EOC signal within 200 msec in phase 3, the meter interprets this as an overload condition and quickly ends phase 3 via a fast time discharge and initiates phase 1 to restart the conversion cycle. The fast time constant introduced into the capacitor discharge circuit aassures that the auto-zeroing integration in phase 1 will start from zero conditions. The overload sense circuit also initiates the development of logic control signals for the overload display.

3.2 OVERALL BLOCK DIAGRAM

As shown in Fig. 3-1, the meter consists of the following major functional sections:

A. Input Signal Conditioner.
B. Tri-Phasic™ Analog-to-Digital Converter (Analog Section).
C. Tri-Phaic™ Analog-to-Digital Converter (Digital Section).
D. Timing Generator.
E. Display.
F. Reference Generator.
G. Power Supply.

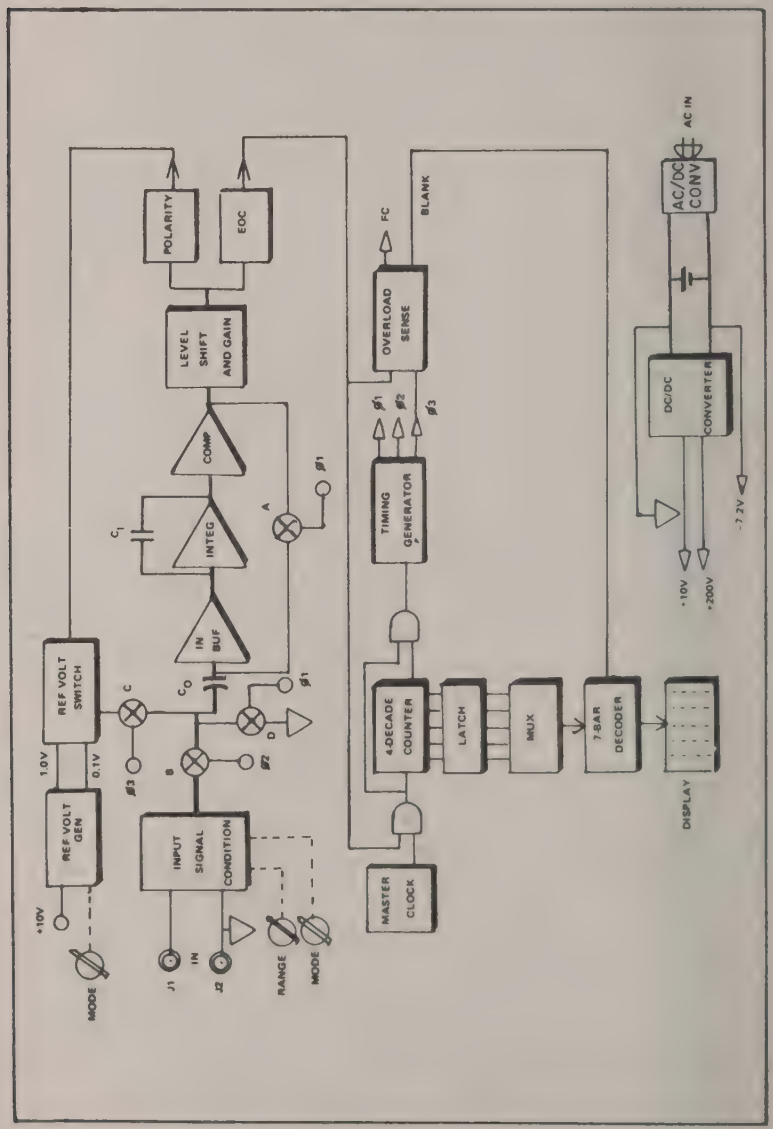


Figure 3-1. Model 1455 DMM Simplified Block Diagram

3.2.1 Input Signal Conditioner

The input signal conditioner receives the connected input voltage or current and develops a scaled voltage output in accordance with the selected meter function and selected full-scale range. The signal-conditioner output is 1.0VDC full scale when the unknown input is a full scale voltage signal on any range or is 0.1VDC full scale when the unknown input is a full scale current signal.

The input signal conditioner section remains linear for the full 100% of overrange input signal values and includes protective elements for overload conditions beyond the specified overload capabilities.

3.2.2 A/D Converter (Analog Section).

The analog section of the Tri-Phasic Analog-to-Digital Converter includes the input buffer stage, the integrator, and the comparator. They function as follows during the three phases of Tri-Phasic operation:

Phase 1

During Phase 1 the analog section automatically zeros the unit to correct for the zero offsets inherent within the analog functioning elements. During this phase, switch A and switch D are closed, removing the conditioned input, while the input to the high input impedance unity gain amplifier is grounded. As a result, the closed loop servos the output of the A/D comparator to near zero. At that time a charge will have been developed across the memory capacitor, C_o, which balances the sum total of all the individual offsets generated within the loop.

Phase 2

At the start of Phase 2, switches A and D open, and switch B closes. In the open position of switches A and D, the analog section retains the offset voltage on memory capacitor C_o as a correcting value which will be combined algebraically with the input signals and the algebraic sums integrated in Phase 2 and Phase 3.

Switch B, which remains closed during Phase 2, connects the input signal conditioner output to the unity gain buffer. Its output is integrated for a fixed time of 100 milliseconds as controlled by the timing generator in the digital control logic. The charge developed on the integrating capacitor C_I is therefore proportional to the magnitude of the input signal, and the output of the high-gain comparator amplifier will be at a saturation level of opposite polarity to the meter input signal.

Phase 3

At the start of Phase 3, switch B opens, removing the conditioned input signal from the unity gain amplifier. At the same time (start of Phase 3), the polarity sense function of the digital section determines the polarity of the comparator output and transmits a control signal to the reference selection switching network thereby connecting the correct polarity of the reference voltages through Switch C to the unity gain amplifier for integration during Phase 3. The reference voltage integrated during Phase 3 decreases the charge on integrating capacitor C_1 until the output of the high gain comparator changes polarity. This change in comparator output polarity indicates end of conversion and is sensed at the output of the level shift and gain stage of the digital section to indicate the start of Phase 1 through the timing generator logic. The cycle repeats. If the charge on C_1 is not reduced to zero in the time interval allowed for full overrange measurements, the digital control logic initiates the overload actions in the multimeter, as explained later. It should be noted that the zero offset is generated and the storage capacitor charge is updated in each conversion cycle. Also, note that the stored voltage representing the corrected zero is introduced into the analog section for both the unknown integration and the reference integration, thereby removing the zero effects from both the charging and the discharging actions on C_1.

3.2.3 A/D Converter (Digital Section).

The digital section of the A to D converter includes the phase timing generator, the comparator output sensing circuit, the counter and code converter circuit. The latter consists of a monolithic chip on which are mounted the four-decade counter, latch, multiplexer, and seven-bar decoder, as well as an internal oscillator and digit selecting counter associated with their operation. The function of the elements on the chip is to convert the time interval needed by the analog section in Phase 3 to reduce the charge of the integrating capacitor to zero into a count which will be displayed as the measure of the input signal. The four-decade counter increments from zero at the start of Phase 3 and builds up a count at the rate of 100 KHz. When the end of conversion signal is developed, incrementing is stopped, and the binary values in the counter are transferred to the latch, where they are held while the multiplexer and decoder translate the binary value into the appropriate lighted segments of the display. Should the signal at the input exceed the 100% over-range value, the end of conversion indication will not be generated before the completion of 20,000 counts. This is the condition for an overload, and the overload sense circuit of the digital section then performs two actions:

a) It develops a blanking signal which blanks all the display digits (not including decimal point and sign) and, in addition,

b) Develops a fast charge signal (FC) which changes the time constant on the integrating capacitor circuit to reduce its charge quickly to zero so that adequate time remains in phase 1 to develop the correct zero correction. If a fast discharge (TC) had not been introduced, it would have been possible for the residual charge to affect the zero correction and to increase the time to recover from overload.

3.2.4 Timing Generator Circuit

The time generator section consists of a master clock, a four-digit counter (the same element as described previously), and a number of logic gates and flip-flops. The function of the timing generator section is to produce the synchronizing control signals which define phases 1 and 2, and in conjunction with the EOC sensing, phase 3. The timing signals are derived from the master clock frequency of 100 KHz which is counted down by the four-digit counter into segments of 100 milliseconds each by gating each 10,000 count carry from the counter. The action of the subsequent logic produces the timing signals in the relationship shown in Fig. 3-2. Fig. 3-2 also shows the charging and discharging of C in these phases.

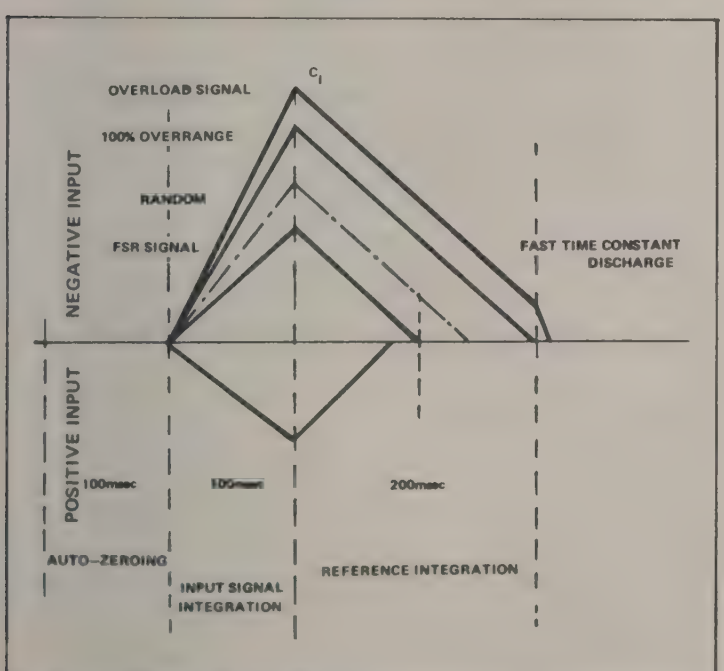


Figure 3-2. Waveforms and Timing Diagram

3.2.5 Display

The display consists of four full decades of seven-segment characters, a fifth element which may take a character of "1" or remain blank, and an element for indicating the polarity of the input signal. The decimal point position is controlled directly by the manual range selection.

3.2.6 Reference Generator

The Iso-polar™ reference generator provides a precise 1.0 or 0.1 volt level to be connected to the analog input for Phase 3 operation. The selection of 1.0 or 0.1 voltage level is accomplished by the mode selection. The Iso-polar action features the development of a precise positive reference voltage and then through precise passive elements and controlled switching obtains positive or negative references with equal magnitudes. The reference generator is powered by the +10 volts received from the DC/DC converter, and also generates the precision +7.2 volts as needed within the unit. The reference voltage generator section also includes the circuitry for ratiohmic measurement connections to be described later.

3.2.7 Power Supply

The power for the meter is obtained from a 7.2-volt battery module which is connected as a negative voltage source, and which is connected as the load of an AC/DC converter (See reference schematic). The transformer input for the converter may be obtained from either 110 or 220 volt sources, and the input configured for the selected source by positioning a slide switch located inside the DMM at the left rear of the main assembly (see Figure 4-2.).

The secondary output is rectified, filtered, and regulated, to deliver -7.2VDC to the battery and to the DC/DC converter. The DC/DC converter is connected to the -7.2 volt battery supply only when a measuring function is selected, and develops nominal +200 volts for the display lamp power and +10 volts for the analog amplifier units. The -7.2 volts for the digital logic and for the analog amplifier units are supplied directly from the battery.

3.3 INPUT SIGNAL CONDITIONING

3.3.1 DC Voltage Signal Conditioning

The circuitry involved in conditioning a DC voltage input is shown in Figure 3-3.

The input at J-1 is the high side of the voltage to be measured, while J-2 represents a common to which all measurements are referred. The illustration indicates the connections made by the front panel circuitry selector switch when in DC Volts mode and for scale "X1". The input is direct for the X1 scale, and is attenuated by the matched precision resistor network in the other scales.

3.3.2 AC Voltage Signal Conditioning

Figure 3-4 illustrates the circuit as connected when the AC voltage is selected by the function switch and when the "X1" range scale is selected at the range switch. As in all measurements, one side of the input is connected through J-2 or the common reference for the input measurement.

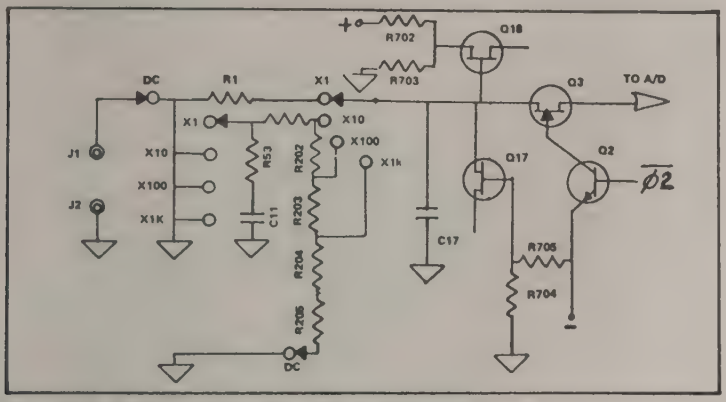


Figure 3-3. DC Voltage Signal Conditioning Schematic

The feedback path around high gain Z1 accomplishes the designed input attenuation as selected by the range switch. The components in this attenuator network are the same as for DCV conditioning, but connected as shown for ACV. The output of Z1 is connected to a half-wave rectifying circuit through a gain stage which is nominally set for a gain of 2.22 so that the average value obtained as a result of the rectification represents the RMS value of an equivalent sine wave input. The filtered output of the rectifying circuit is the input to the A/D converter section. Thereafter, the circuit operation is the same as for measuring DC voltage, while the displayed result is in terms of the RMS value of the AC input.

3.3.3 Resistance Input Signal Conditioning

The resistance value to be measured is connected across input terminals J_1 and J_2, and the simplified schematic illustration of Figure 3-5 is drawn to indicate the circuit connections when in resistance measurement mode.

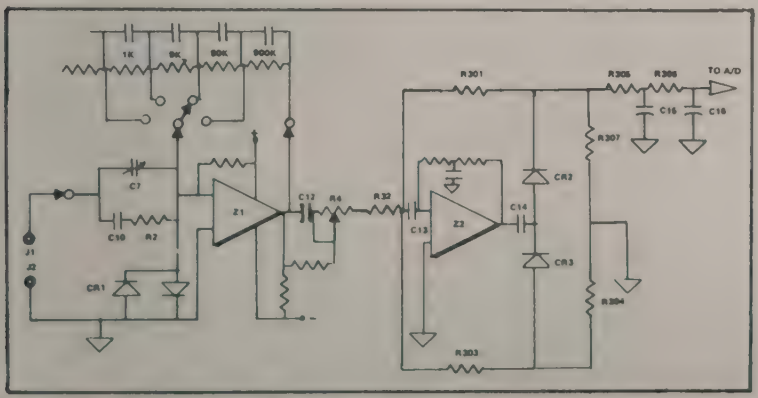


Figure 3-4. AC Voltage Signal Conditioning Schematic

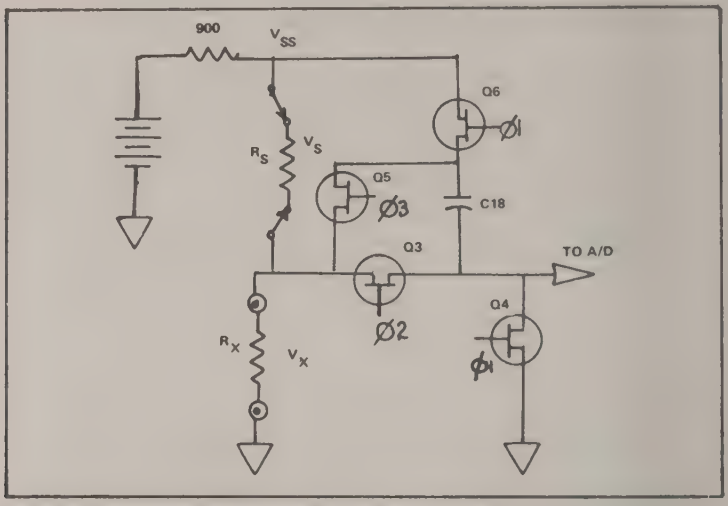


Figure 3-5. Resistance Measurement Signal Conditioning

In the Ratiohmic™ technique shown in the simplified schematic of Figure 3-5, the current I, passing through the series combination of the selected standard resistance Rs and through the unknown resistance R_X generates the voltage drops identified in Figure 3-5 as V_X and V_S.

The values of voltage connected to the A/D buffer input depend upon the controlled switch closures of Q3, Q4, Q5, and Q6. During Phase 1, Q6 and Q4 are closed. This provides a charging path for capacitor C18 which charges to the potential V_{SS} equal to $V_S + V_X$. During Phase 2, Q3 is closed and the voltage V_X across R_X is connected to the A/D buffer input.

During Phase 3, switch Q5 is closed and this action places the high side of the capacitor at the V_X level while the low side is connected to the A/D buffer input. The low side is then $V_S + V_X - V_X = V_S$. The integration proceeds until the charge on the integrating capacitor (not shown in Fig. 3-5) is reduced to zero as in voltage conversion. The A/D converter measures the ratio of $V_X/V_S = R_X/R_S$ and displays the result calibrated in kilohms according to the selected full scale range.

3.3.4 DCmA Input Signal Conditioning

Fig. 3-6 is a simplified block schematic of the circuit as connected when the function mode switch is in the DCmA position and when the range switch is in the X1 position. The input is connected across J1 and J2, with J2 functioning as the common reference for this and for all measurements.

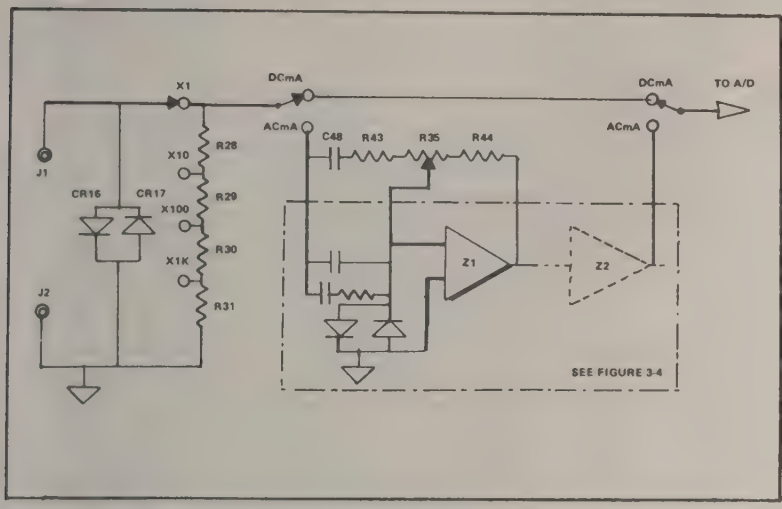


Figure 3-6. Current Signal Conditioning Schematic

The network R101, R102, R103, R104 forms a precision shunt for scaling the input current to an appropriate value of input AC voltage depending upon the scale selected. The output of the shunt network is the scaled DC voltage which is connected to the A/D converter input. Thereafter, the circuit performs exactly as for DC voltages.

The protection devices for overload in the DCmA mode are CR101 and CR102, a pair of diodes whose breakdown voltages provide a threshold to limit the input signal to 2 volts.

3.3.5 ACmA Input Signal Conditioning

Fig. 3-6 also illustrates the connections of the function mode switch for the ACmA measurement mode. As illustrated, the AC milliampere input signal is first connected to the shunt network becoming a voltage input which is then scaled in the feedback path of Z1 and Z2, the two stages of amplifier and rectifier as described for the AC voltage signal conditioning. The scaled DC signal is then connected to the A/D buffer input.

3.4 TRI-PHASIC A/D CONVERTER (ANALOG PORTION)

The simplified schematic of Fig. 3-7 illustrates the operation of the analog portion of the Tri-phasic analog-to-digital converter. This portion consists of three major operational elements: (1) unity gain buffer amplifier Z4A, preceded by matched high impedance input FET's Q8A and Q8B; (2) high-gain operational amplifier Z4B, connected as an integrator with integrating capacitor C20 in the feedback path, and (3) high-gain comparator Z5 driving to saturation for a small difference in potential between the integrator output and the ground reference. During phase 1, the three

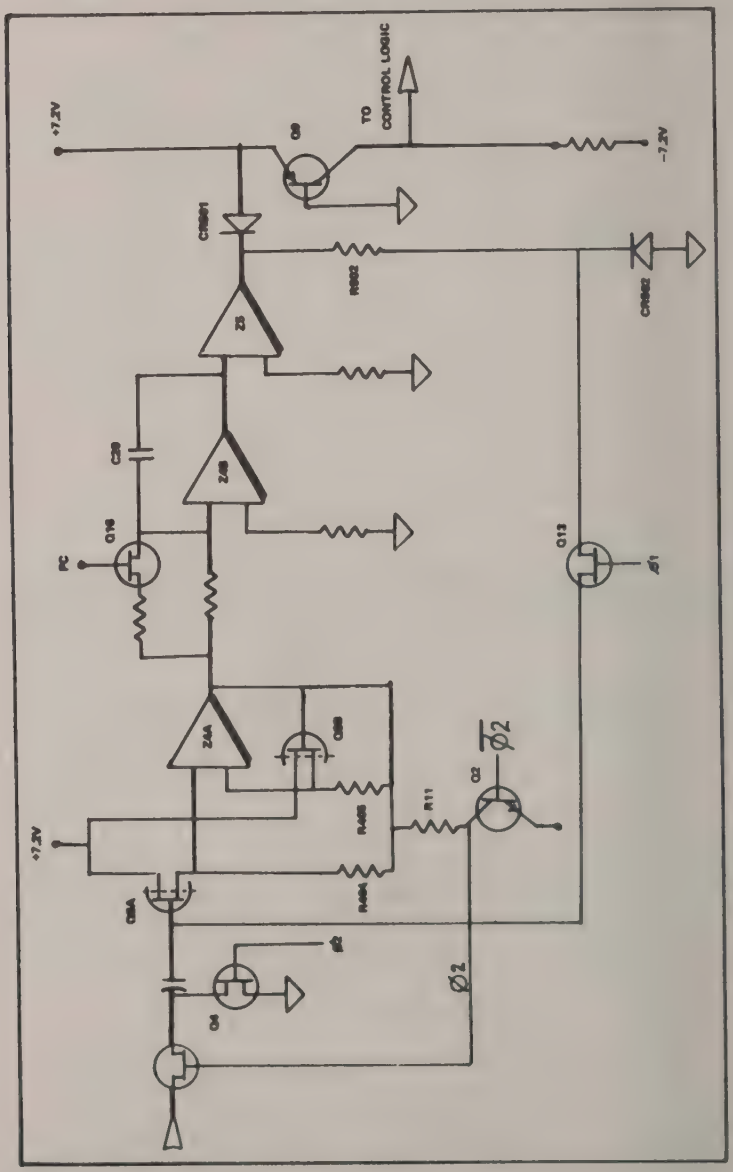


Figure 3-7. A/D Converter (Analog) Simplified Schematic

elements are connected in a closed loop by FET switch Q13. The comparator output is followed by a level shift and gain stage, consisting of diode CR501 and transistor Q9 for proper level and drive values in subsequent logic circuitry.

As controlled by signals from the digital portion of the converter (to be described later) the analog portion (1) automatically updates the zero correction, (2) integrates the conditional input (scaled according to the function selected so that 1.0 volts is full scale for voltage measurements and 0.1 volts for current or resistance measurements) and (3) integrates the reference voltage of appropriate polarity and full scale magnitude.

3.5 END OF CONVERSION AND POLARITY SENSING

The digital control logic for sensing EOC and input signal polarity is illustrated in the simplified schematic of figure 3-8.

At the start of phase 3, the state of flip-flop Z7B indicates the polarity of the input signal integrated during phase 2. If the unknown input signal were negative, the D input to Z7B would be at the ground level; if the unknown meter signal were positive, the D input to Z7B would be at the −7.2 volt level. At the phase 3 clock pulse to flip-flop Z7B, the D input is transferred to the Q output, and the control level appears on the appropriate polarity switch-selecting line. As shown in the illustration, phase 3(−) implies selecting a positive reference for a negative input signal, and phase 3(+) implies selecting a negative reference for a positive meter input signal.

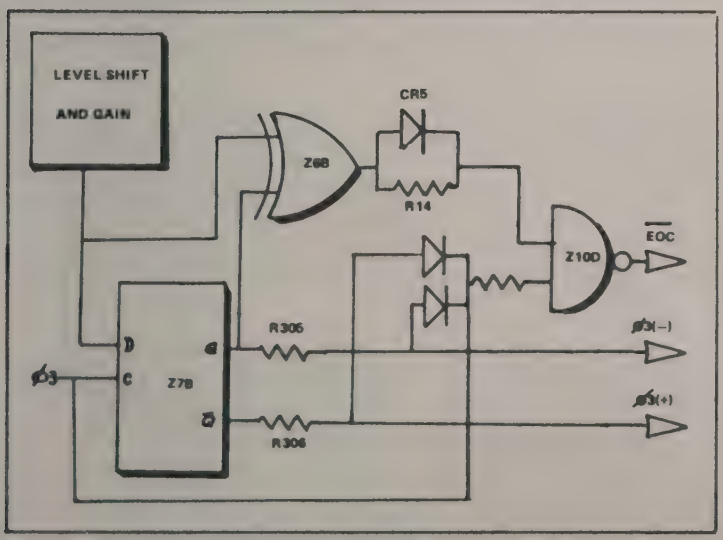


Figure 3-8. EOC and Polarity Sensing Schematic

One or the other of Z7 outputs must be a high level signal input to gate Z10D while the other input signal to Z10D comes from exclusive OR gate Z6B. Because both inputs to Z6B are the same polarity at the start and during phase 3, the output of Z6B is at low level. As soon as the polarity of the comparator output changes, gate Z6B responds by delivering a high output level, and thereby causes gate Z10D to issue a low level signal which signifies the end of conversion, EOC.

3.6 A/D CONVERTER (DIGITAL SECTION) AND TIMING GENERATOR

The digital logic section of the Tri-phasic A/D converter instruments the programming control functions to signal the start of Phase 1, Phase 2 and Phase 3 of each conversion cycle. Phases 2 and 3 control signals are derived from clock generated pulse trains, while Phase 1 may be initiated by the end of conversion or from the clock chain if input is an overload signal. The digital logic section also generates the control signal for selecting the appropriate polarity of reference voltage for Phase 3 integration and for display purposes.

The timing generator consists of a stable tuned free-running clock oscillator in the DC/DC Converter whose gated output drives a 4-decade counter and from which the digital control logic develops the program control signals.

Both the digital section and the timing generator functions are illustrated in the simplified block schematic of Figure 3-9. The operation of the circuit illustrated in this block diagram may be understood by tracing the development of the waveforms as shown in the timing waveforms of Figure 3-10.

The change in output polarity from the comparator occurring in Phase 3 is the indication of end of conversion, EOC. It is converted to a negative-going pulse at the output of Z10D (figure 3-8), and serves two functions:

a) The leading, negative-going edge blocks the clock output, preventing a count pulse from further changing the value in the counter.

b) The positive going edge enables the transfer from the counter to the latch of the value in the counter at that time. (See Reference Schematic).

The $\overline{\text{EOC}}$ pulse is also gated by exclusive OR gate Z6A to reset flip-flop Z8B at the DR input. This action causes the Q output of Z8B to go low, and, in combination with the Phase 2 signal at the input to Z6E, generates the digital control signal for the start of Phase 1. Note, in Fig. 3-10, that both $\overline{\text{Phase 2}}$ and Phase 3 signals are high during Phase 3, and thus the exclusive OR gate Z6E remains low until one of the inputs goes low.

Should the counter reach a second carry while Phase 3 is in process, indicating an overload condition, the digital control logic will respond as follows

a) The second carry causes Z8B to change states (rather than be reset by EOC). This action produces Phase 1 control signal through gate Z6E.

b) The gate formed by R40 and CR18 produces a high level output for the FC signal. The FC control signal activates FET switch Q16 (figure 3-7) and introduces a fast time constant in the integration path in order to reduce the remaining charge on integrating capacitor C20.

c) The outputs of Z9A and Z9B will also cause flip-flop Z7A to generate the overload blanking control signal connected to the 7 segment converter of the display logic.

DISPLAY* 3.7

The display comprises two segments DS-1 and DS-2, providing the capabilities for 4 full decade digits, a most significant digit which is "1" or blank, automatically selectable positive or negative polarity indication, and five selectable decimal point indications.

The decimal digits are made up of appropriate combinations of seven segments driven one digit at a time by a multiplexed BCD to 7-segment converter logic. The converter is synchronously connected to the latched values at the same time +200V power is applied to the selected digital display position. The counter, latch, multiplexer, and 7-segment converter, as well as the scanning oscillator, digit select logic and buffer for control of the high voltage are all contained in the LSI module.

The decimal point selection is made directly to the display by the manually selected range switch. The selected range causes the appropriate decimal point control line to be grounded, lighting that decimal point display. The polarity indication is similarly actuated directly at the display, but by the polarity select digital control signals.

The blanking action is effective through the code converter, and operates on the decimal display digits. The polarity and the decimal point indications are not affected by the overload control.

When measuring current, the mode selector switch acts to block the application of high voltage to one decade, permitting only a 3 1/2 digit display for measuring current on any range scale.

*See Fold-Out Reference Schematic

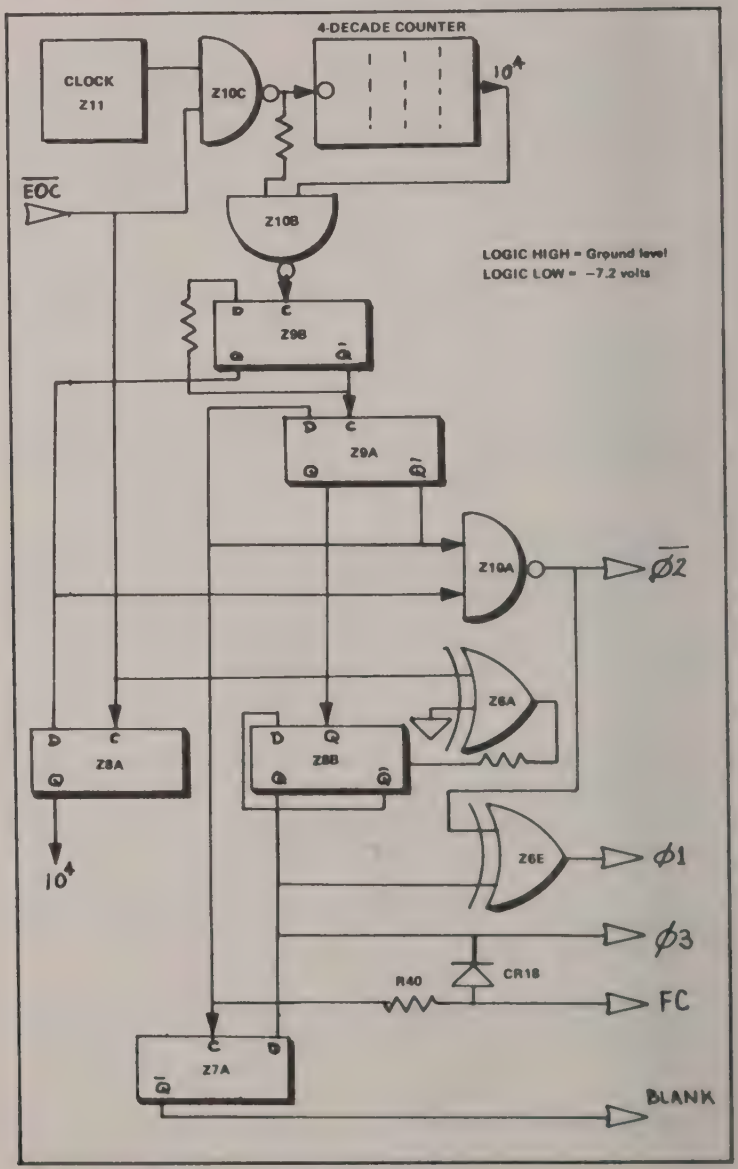


Figure 3-8. Digital Control Logic Block Diagram

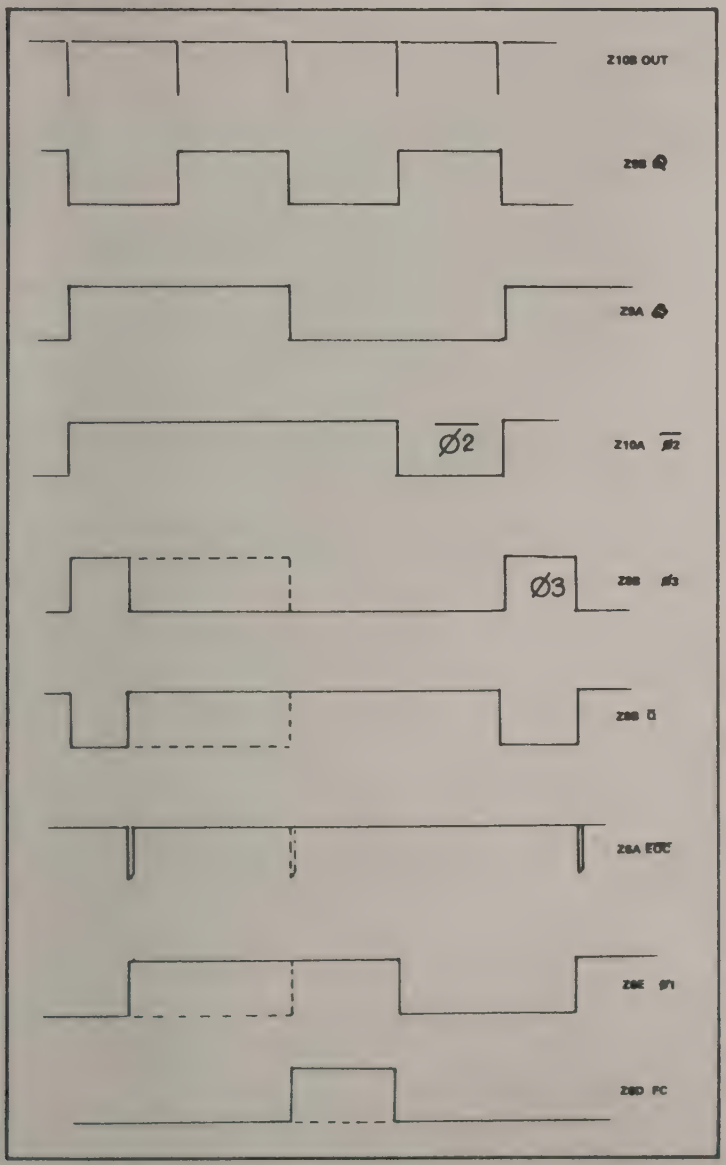


Figure 3-10. Digital Timing Diagrams

3.8 ISO-POLAR REFERENCE GENERATION

The Iso-polar reference generation is accomplished as illustrated in the simplified schematic of Figure 3-11. The generation of correct magnitude of reference voltage for resistance measurements, and the generation of digital control signals $\phi 3(-)$ and $\phi 3(+)$ for negative or positive meter inputs, respectively, have been described previously.

The simplified circuit schematic indicates the operation in two major segments:

1) Generation of a zener-controlled servoed positive reference level, calibrated for full scale by R10.
2) Action by purely passive components to apply either positive or negative levels as required.

Operational amplifier Z3 in the servo loop controlled by Zener CR4, produces a voltage level of 1.0V across the precision resistor network R6 and R7, so that 1.0V or 0.1V is selected for voltage or current measurements, respectively (0.1V is also used for resistance measurements as explained earlier).

During Phase 1, while the auto-zeroing action is in process, C18 is charged to the value of selected magnitude (1.0V or 0.1V) by the charging path formed by closed FET switches Q6 and Q4.

During Phase 2, while the unknown meter input is being integrated, the charged capacitor C18 is removed from the circuit.

At the start of Phase 3, if a negative meter input has been sensed, then switch Q7 is closed by $\phi 3(-)$, connecting the positive reference value to the A/D input (in series with the zero correction value stored on C19 during Phase 1.)

If a positive meter input has been sensed, then switch Q5 is closed by 03(+), connecting the high side of C18 to ground reference level. The low side of C18 is then the negative value of reference voltage and is connected to the A/D input as explained above.

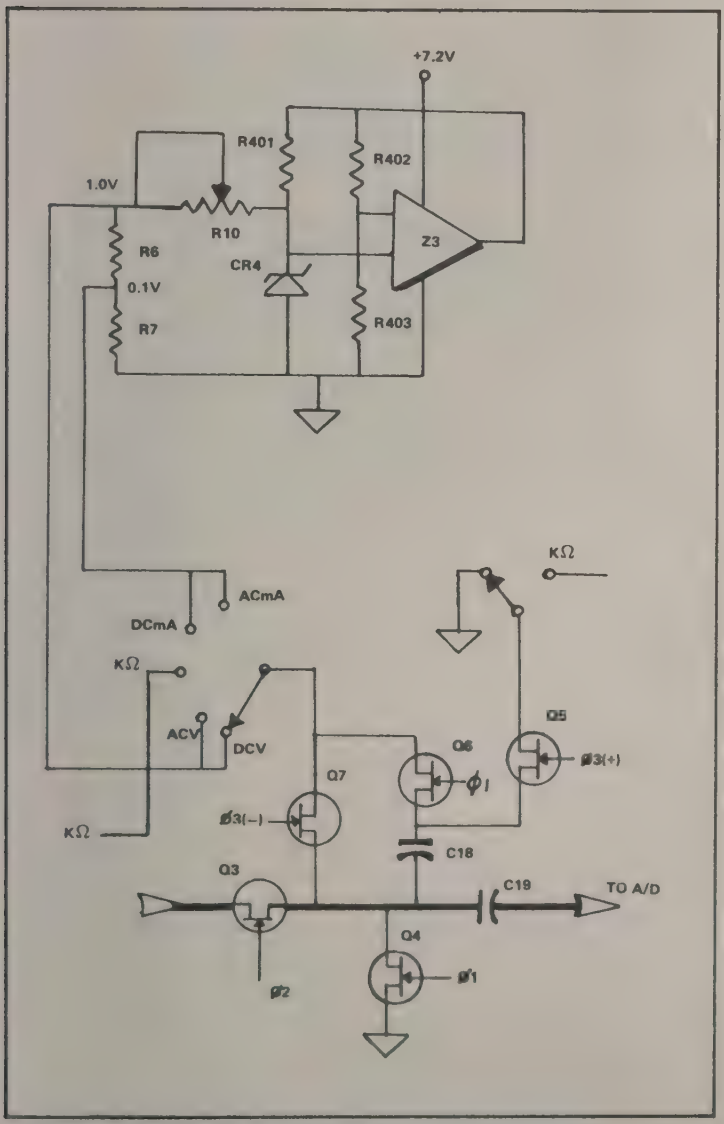


Figure 3-11. Iso-Polar Referencing Voltage Generation Schematic

3.9 POWER SUPPLY

The AC input, fused by F2, is connected to the primary windings of transformer T2 through slide-selector switch S3 which connects the primary windings in series or parallel for 230V or 115V inputs, respectively. The T2 secondary output is rectified by CR24 and CR25 , providing a nominal 7.2 volts across the battery. The positive terminal of the battery module connected to analog ground so that the supply voltage of −7.2V is available for analog curcuit operation and digital logic without further conditioning.

As shown in the detailed schematic at the back of the book, the DC/DC connector provides additional filtering of the −7.2V, then develops nominal +200V to power the display indicators, +10V for the analog amplifier and input circuits, and a chain of clock pulses for timing and measuring as described later. Logic supply of −7.2V and the −7.2V needed for analog circuit operation are obtained from the DC/DC converter input side.

The DC/DC converter converts the -7.2V DC input to an AC signal by the oscillator consisting of Q14 and Q15 and phase shifting network R22 and C27. The resulting AC signal drives primary of transformer T1; one secondary winding output is full-wave rectified and filtered to provide the +10V supply; the other secondary winding output is full wave rectified to provide the +200V for the display indicators.

Chapter 4

MAINTENANCE

4.1 GENERAL

CAUTION

The Model 1455 Multimeter is covered by a one-year warranty and should be referred to the factory for maintenance within the warranty period. Attempts to make any extensive repairs within the warranty period may invalidate the warranty. If repairs are needed after the warranty period, only qualified technicians should attempt to effect such repairs and should use test instruments and standards calibrated within the accuracy and tolerances of the specifications.

4.2 TROUBLE-SHOOTING FLOW CHART

Should the meter performance indicate a possible need for repair, a well-defined strategy should be used to isolate the cause of trouble. This is illustrated in Figure 4-1. It indicates a sequence of steps and defines a program of actions in terms of standard symbols based on a philosophy of *positive* maintenance. The positive approach isolates to the faulty sections by verifying proper operation of the remaining instrument sections.

4.3 TEST POINTS

The test sequences identified in the chart of figure 4.1 are described in step-by-step detail in the paragraphs that follow. In performing the tests detailed in these paragraphs, the maintenance technician is directed to make measurements at designated test points which have been placed at significant portions in the circuit. The special test points are identified by E-reference numbers, and their locations on the printed circuit board are shown in figure 4.2. Other test points designated in the test procedure paragraphs may be pin terminals of circuit components, and technicians should refer to component data sheets for the pin terminal locations as well as to figure 4.2. Use caution in attaching test leads to avoid accidental shorting of adjacent components. The use of EZ Mini Hook ®, or equivalent is suggested to aid in making good connections.

A separate test point for measuring battery charge has been brought out to the rear panel (See Figure 2-2). See paragraph 2.4.2 for test procedure.

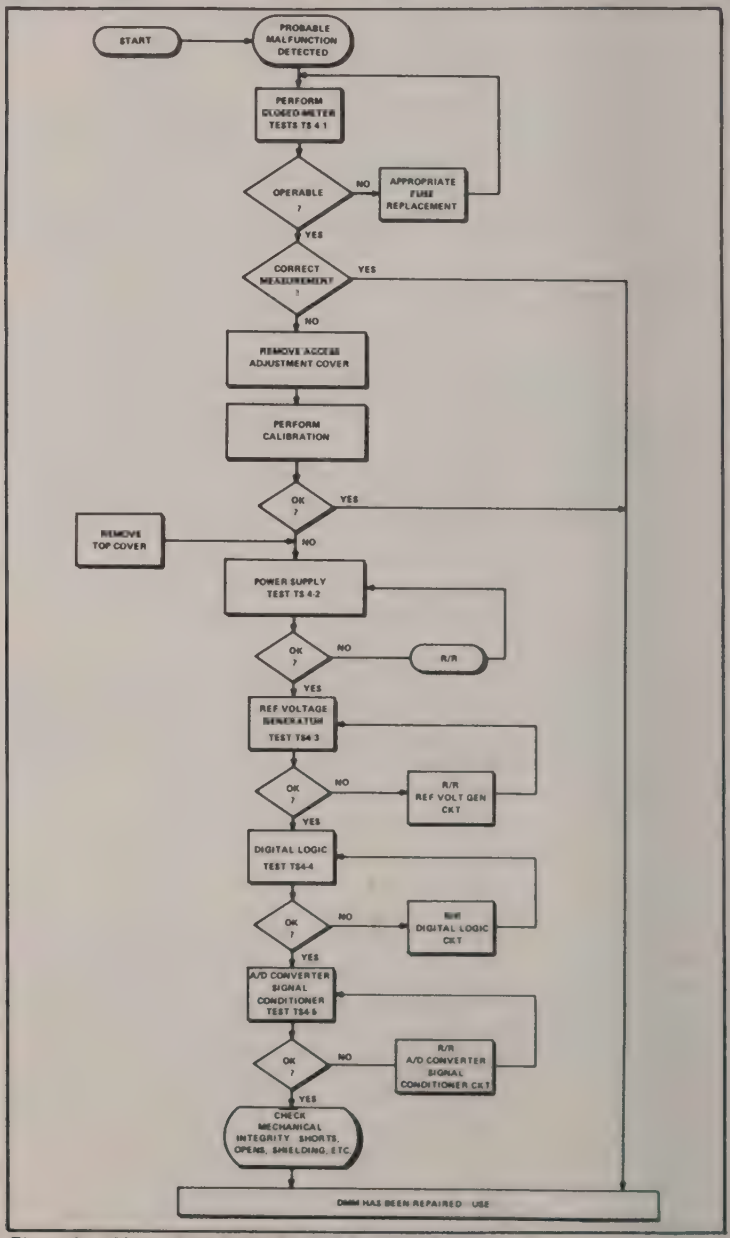


Figure 4-1. Model 1455 DMM Trouble Shooting Strategy

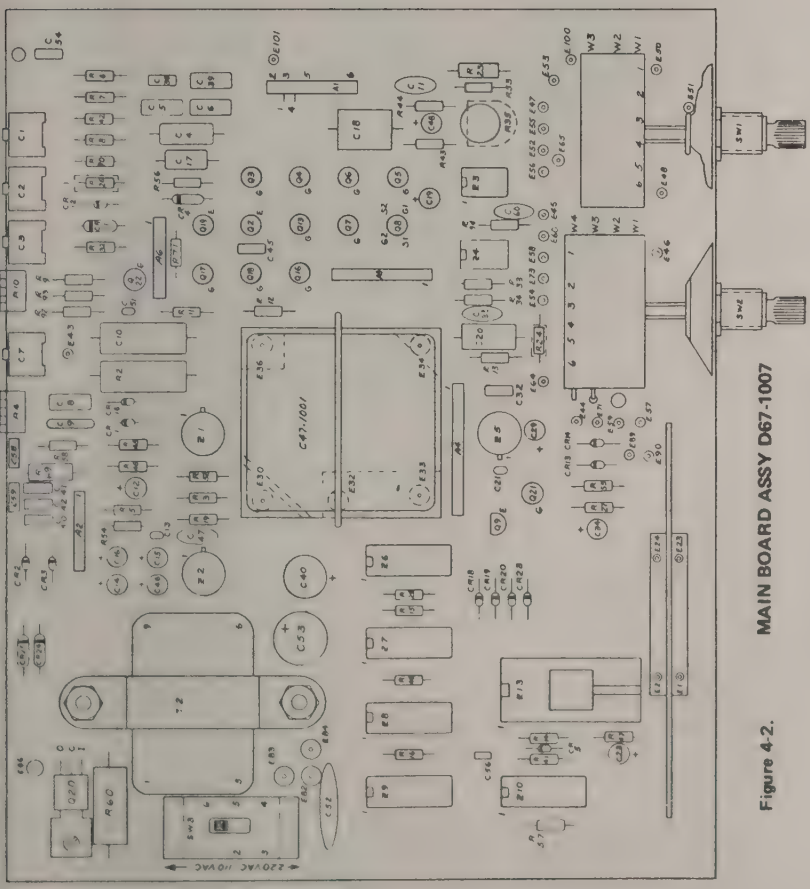
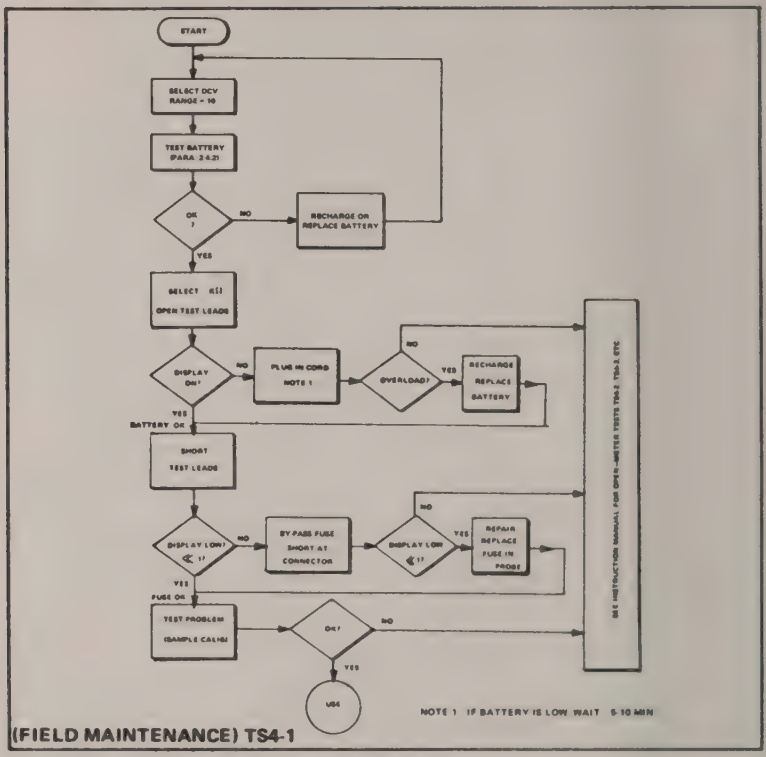


Figure 4-2. MAIN BOARD ASSY D67-1007



(FIELD MAINTENANCE) TS4-1

4.4 CLOSED-METER TESTS (FIELD MAINTENANCE) TS4-1

The first test sequence is performed with the "cased" meter. The sequence is fully detailed in the illustration of TS4-1.

4.5 OPEN-METER TEST/MAINTENANCE

4.5.1 General

If the multimeter does not perform correctly after the tests of TS4-1 are satisfactorily completed, then it is likely that the meter must be recalibrated, repairs to an internal assembly are required. The sequence of such tests is indicated in the overall strategy of Figure 4-1, and is identified by a TS number for further reference. Each test sequence paragraph includes the designation of test points, the indications of proper performance, the circuits that are checked when proper performance is observed, and the circuits that should be examined in greater detail when indications of improper performance are recorded. Refer to the fold-out schematic in the back of this manual for complete circuit details, and to Chapter 5 for replacement parts identification.

4.5.2 Removing Top Cover

The top cover of Model 1455 DMM is held in place by two fastening screws to the top of the rear panel and by a lip over two dimples of the front panel. To remove the top cover, merely remove the two rear fastening screws and lift up. All components are mounted on the top of the main PC-Board assembly, and are accessible, once the top cover is removed. Figure 4-3 is a layout schematic, identifying the components and test stand offs, including the components under the DC/DC Converter.

4.6 Test Equipment

Test instruments and reference standards needed for the trouble shooting analysis should have the following characteristics:

Parameter	Range	Accuracy	Measure/Generate * M/G
DC Voltage	–10V to +10V	±0.1%	M/G
	+200V	±1 %	M
AC Voltage	100KHz 1 VRMS		
	20KHz 200 VRMS	±0.1%	M/G
	100 VRMS		
	10 VRMS		
	1 VRMS		
Timing Waveforms	Oscilloscope 5 MHz BW	±5%	M
Resistance	0 to 10 MΩ		M/G

*Measure = indicates test instrument, Generate = indicates source instrument

4.7 POWER SUPPLY TEST, TS4-2

a) Select KΩ Mode and 10MΩ Range positions
b) Check for the indicated voltages at the test points shown below:

Test Points*	Measure Value
E 36	+10.0V ±1V
E 30	Battery (-7.5V nom)
E 33	+190 to +230V

*Measurements are made with respect to E69

c) If all readings are correct the input Power Supply circuit and the DC/DC converter are operating satisfactorily. An incorrect reading may result from a short circuit in one of the boards driven by the power supply or by a failure within the DC/DC converter, or power input.
d) Turn off power to meter by positioning Function switch of OFF. Carefully unplug the DC/DC Converter assembly.

WARNING

The +200V supply to terminal E33 from the Converter will remain HOT'. Handle with care. Do not place on conducting surface.

e) Ground the +200V and the +10V supplies.
f) Measure the resistance to ground at E.33. If zero (essentially a short circuit) then the Display assembly is suspect
g) Measure the resistance to ground at E36. If zero (essentially a short circuit) then one of the three analog modules Z3, Z4, or Z5 is suspect.
h) Measure the resistance to ground at E30. If zero, or infinity then one of the digital logic modules is suspect.
i) If the resistance measurement values are satisfactory but other measurements are not, then replace the DC/DC Converter with a new one.

NOTE

Correct power supply readings do not always imply correctly driven loads.

4.8 REFERENCE VOLTAGE GENERATOR: TS4-3

a. Select KΩ Mode
b. Measure 1.0000V±0.0001V at R6, R8 junction
c. Attempt to adjust to correct value by R10.

If correct proceed to 4.9. If correct value cannot be obtained by R10 adjustment, then trouble shoot voltage reference generator circuit. See details in fold-out.

4.9 DIGITAL LOGIC: TS4-4

NOTE

In all logic timing waveforms, high levels are at ground potential; low levels are at −7V potential.

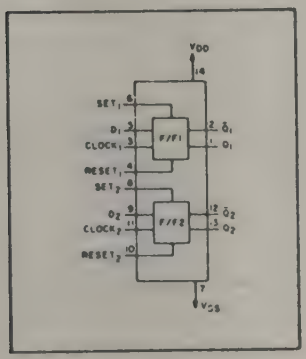
4.9.1 Basic Logic Modules

Model 1455 DMM utilizes three basic logic IC's in its design. Each one is a COS/MOS (monolithic silicon) type unit. They are:

a) NAND Gates
b) Exclusive OR Gates
c) D-Type Flip-Flops

Their schematic representations, pin-terminal designations and logic truth tables are defined below for assistance in trouble shooting and fault isolation.

Dual D-Type FLIP–FLOP



TRUTH TABLE

CL*	D	R	S	Q	Q̄
↗	0	0	0	0	1
↗	1	0	0	1	0
↘	x	0	0	Q	Q̄
x	x	1	0	0	1
x	x	0	1	1	0
x	x	1	1	*	*

NO CHANGE

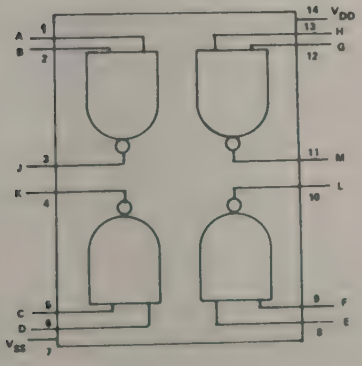
* = INVALID CONDITION

** = FF1/FF2 TERMINAL ASSIGNMENTS

↗ = LEVEL CHANGE

x = DON'T CARE CASE

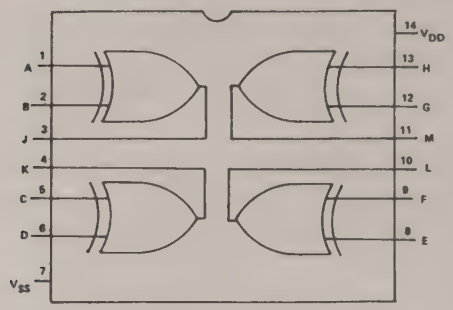
C /MOS Quad NAND Gate



TRUTH TABLE

IN 1	IN 2	OUT
0	0	1
0	1	1
1	0	1
1	1	0

COS/MOS Quad Exclusive OR Gate



TRUTH TABLE

IN 1	IN 2	OUT
0	0	0
0	1	1
1	0	1
1	1	0

4.9.2 Clock

a. Select DCV measuring mode at the Mode Switch.
b. Use an oscilloscope to observe the clock output waveform of approximately 100 KHz at E32. (Note: accurate 100 KHz signal is required for proper multimeter operation, but that adjustment can be made later, using potentiometer R18, accessible through hole in the DC/DC Converter cover).

If frequency is within tolerance (± 1%), the clock circuit is functioning correctly. If not, trouble shoot the clock circuit in the DC/DC converter Module.

4.9.3 Phase Timing Signals

a) Jumper a connection from Z7B pin 13 to the input, pin 6, of Z6B. This will simulate an overload input signal.
b) Use an oscilloscope to trace the waveform generation in the digital logic units and verify the waveforms of figure 3-10. See the detailed schematic at the back of the book for IC pin terminals and for detailed trouble shooting.
c) Observe the overload display on the front panel. If not proper, trace signal trhough chip.

4.9.4 Polarity Logic

a) Ground the input to Z6B. This simulates a negative input signal.
b) Observe the negative polarity sign on the display.
c) Replace jumper connection of a) above with a jumper connecting -7.2V to the input pin 6 of Z6B. This simulates a positive input signal to the meter.
d) Observe the change in polarity sign from negative to positive.

If proper performance is not observed, check the polarity flip-flop circuitry and the display circuitry. (See detailed reference schematic).

4.10 A/D CONVERTER & SIGNAL CONDITIONERS: TS4-5

4.10.1 General

The performance of the A/D Converter and the signal conditioners are now checked at the output of buffer amplifier Z4A, pin 1, so that the measuring instrument will not load down the signal. The procedures require the introduction of test signals at the input to the multimeter and checking performance at two places:

a) At the display. Observe readings; check that they are correct.

If satisfactory, then that mode of measurement range scale attenuation, A/D converter, and display segment decoding and indicating are all satisfactory.

b) At the output of Z4A. (If display is not correct).

If satisfactory, then the malfunction may be in the display circuitry, character segment, or in the Z4B and Z5 stages of the A/D Converter.

4.10.2 Fault Analysis Logic

If the output of Z4A is not correct, then judicious cycling of range scales and measurement modes may be able to isolate malfunctioning elements. For example, if a correct value is obtained for only one polarity (and incorrect for the other), then the reference voltage switching circuits should be checked. Malfunctioning character segments may be detected by varying the input over a range, and observing the display. If DC inputs are correct but AC values are not correct, then the malfunction is probably in the AC to DC converter circuitry.

If Both AC and DC voltage measurements are correct on all ranges, but current measurements are incorrect, then the trouble may be isolated to the current shunt. If some DC measurements are correct and some are incorrect, then one may suspect the input attenuator network.

4.11 PROGRAMMED TROUBLE–SHOOTING FLOW DIAGRAMS

Figures 4-4 and 4-5 are step-by-step programs for fault isolation which may be used to supplement the instructions in the previous paragraphs. These trouble-shooting procedures should be performed by qualified technicians because they include the removal and replacement of soldered connections in order to carry out the program to the isolation of faulty components and circuit elements.

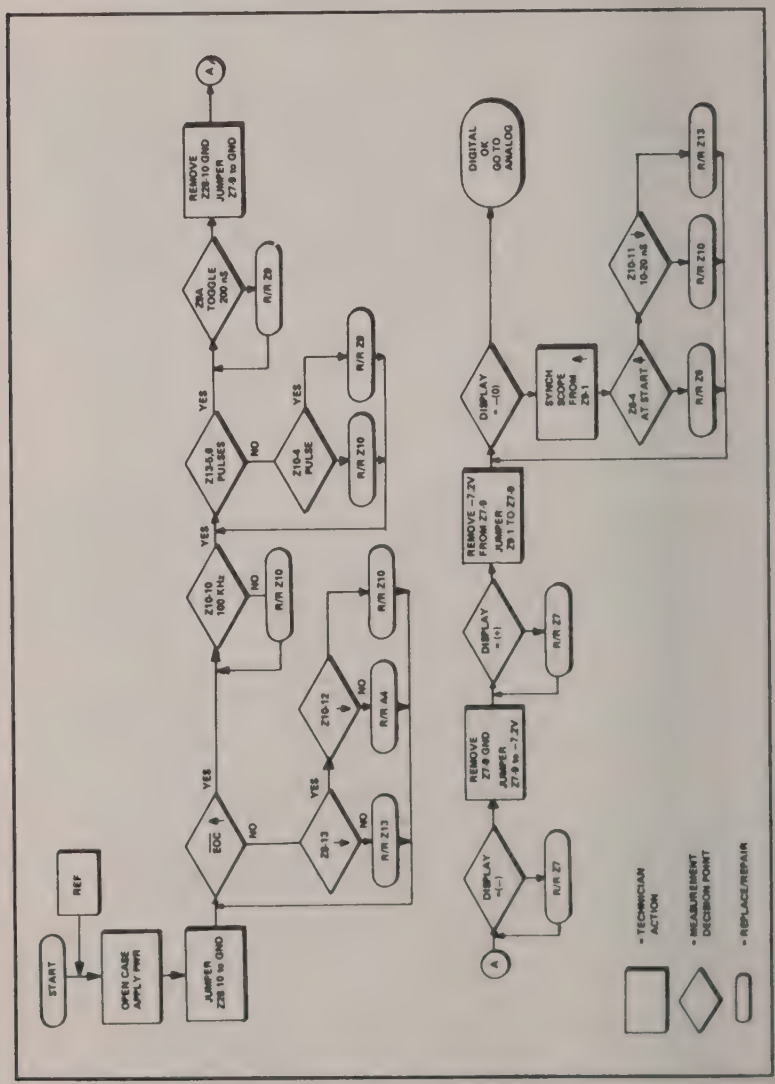


Figure 4-4. Trouble Shooting the Digital Portion of Model 1455

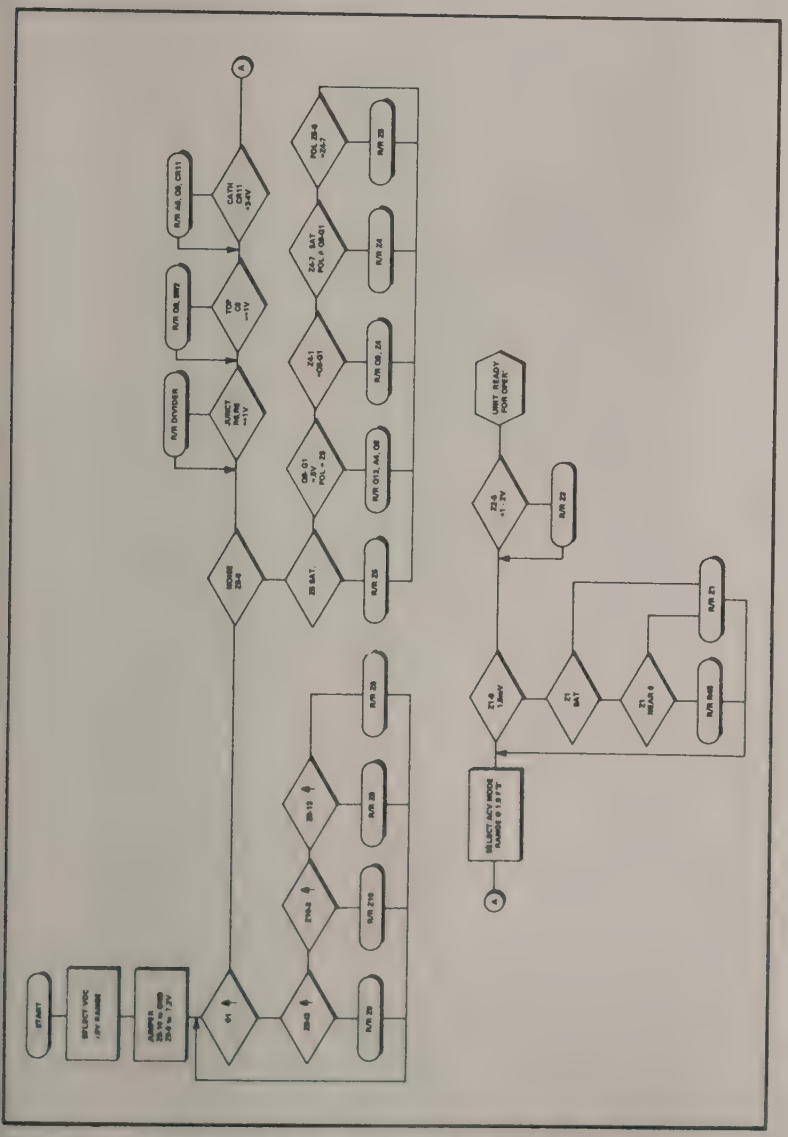


Figure 4-5. Trouble Shooting the Analog Portion of Model 1455

NOTES

Chapter 5
PARTS LISTS
(Replaceable Parts)

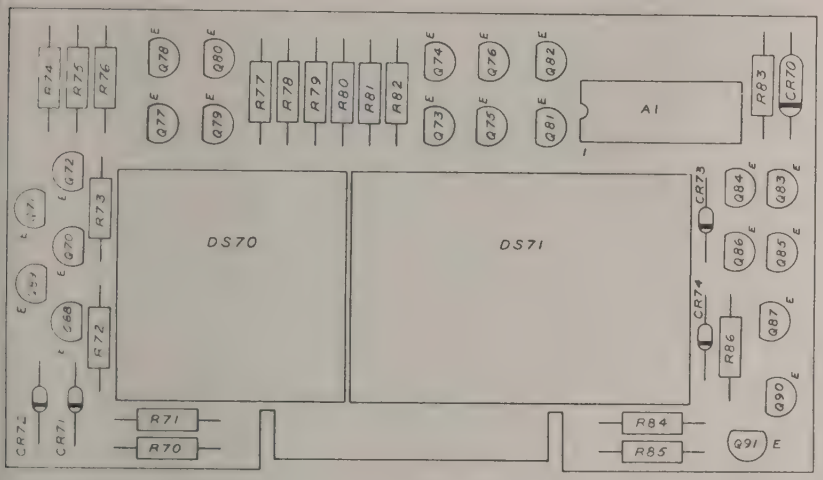
5.1 MAIN BOARD ASSEMBLY, D67-1007 (See Figure 4-2)

REF. DESIG.	DESCRIPTION	PART NUMBER
A1	Network, Input Attenuator	22-48-1009
A2	, Resistor	22-48-1004
A3	, Resistor	22-48-1003
A4	, Coupling	22-48-1008
A6	Network, Resistor	22-48-1011
	DC-DC Converter Assembly	C47-1001
C1	Capacitor, Variable 2-8pF	23-810004
C2, C3, C7	, Variable 10-60pF	23-810003
C4	, .018μF, 50V, 2%	23-550102
C5	, 150pF, 500V, 5%	23-311015
C6	, 1800pF, 500V, 5%	23-312018
C8	, 12pF, 1000V, 10%	23-111002
C9	, 10pF, 1000V, 10%	23-110003
C10	, .1μF, 400V, 20%	23-240001
C11	, .001μF, 1KV, 20%	23-118202
C12, C29, C34, C48	, 15μF, 10V, 20%	23-441003
C13, C51	, 220pF	23-140029
C14	, 47μF, 6.3V, 20%	23-441053
C15, C16, C23, C46	, .47μF, 35V, 20%	23-441051
C17	, .056μF, 50V, 10%	23-510020
C18	, 2μF, 50V, 10%	23-510002
C19	, 100μF, 3V, 20%	23-442050
C20	, 1μF, 50V, 10%	23-510001-A
C21, C50, C56	, 10pF, 50V, 20%	23-140013
C32	, 2pF, 50V	23-310001
C30	Capacitor, .022μF, 50V, 10%	23-140100
C33, C47	, .1μF, 12V, 20%	23-118206
C39	, Final Adjust, DM15	
C40	, 68μF, 15V, 20%	23-442004
C41, C42	, 4.7pF, 50V, ±0.25pF	23-140101
C45, C54, C58, C59	, Final Adjust	
C52	, .02μF, 1KV, 20%	23-118008
C53	, 330μF, 35V	23-620003
C60	Capacitor, .01μF, 150V, +60-40%	23-111006
CR1-CR3, CR5, CR12, CR16, CR18-CR20, CR23	Diode, IN4148	24-110001
CR4	Diode, REF Zener	24-48-1001
CR11, CR24, CR25	Diode, IN4004	24-104004
CR13, CR14	Diode, Low Leakage Rectifier	24-48-1013
Q2	Transistor, 2N3903	24-233903
Q3, Q13, Q16	, FET, Blue or Yellow Dot	24-48-1014-02OR-05
Q4	, FET, White Dot	24-48-1074-02
Q5, Q6	, FET, Green Dot	24-48-1014-03
Q7	, FET, Blue Dot	24-48-1014-02
Q8	, FET, Dual	24-48-1012
Q9	, 2N3905	24-243905
Q17, Q18	, FET, Yellow or Grn. Dot	24-48-1014-03OR-05
Q20	Transistor, 78M08UC	24-308M08

5.1 MAIN BOARD ASS'Y (CONTINUED)

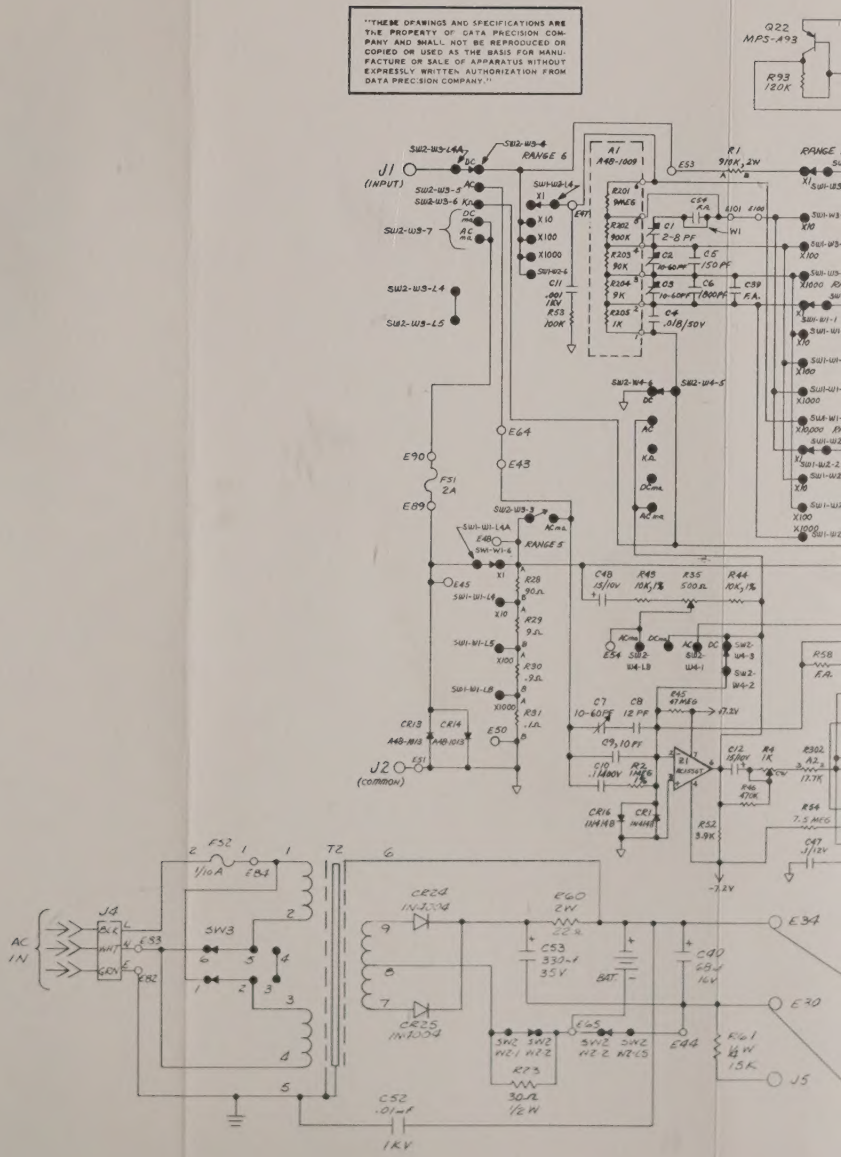
REF. DESIG.	DESCRIPTION	PART NUMBER
Q19, Q22	Transistor, Gen. Pur., PNP	24-240A93
R1	Resistor, 910K, 2W, 5%, C.C.	22-059149
R2	, 1 MEG, 1W, 1%	22-48-1048
R3, R5, R34	, 1 MEG, ¼W, 5%, C.C.	22-021059
R4	, Variable, 1000Ω, 20%	22-670102
R6	, 9K, (Note 1)	22-48-1005-1
R7	, 1K, (Note 1)	22-48-1005-2
R8	, 52K, (Note 1)	22-48-1005-3
R9	, Final Adjust, RN55C	
R10	, Variable, 200Ω, 10%	22-674201
R11, R12, R19	, 27K, ¼W, 5%, C.C.	22-022739
R13	, 47Ω, ¼W, 5%, C.C.	22-024709
R14, R46	, 470K, ¼W, 5%, C.C.	22-024749
R15, R16	, 2.7 MEG, ¼W, 5%, C.C.	22-022759
R24, R53	, 100K, ¼W, 5%, C.C.	22-021049
R25	, 18K, ¼W, 5%, C.C.	22-021839
R26	, 39K, ¼W, 5%, C.C.	22-023939
R27, R40, R41, R47	, 15K, ¼W, 5%, C.C.	22-021539
R28	, 90.00Ω, (Note 2)	22-68-1015-2
R29	, 9.000Ω, (Note 2)	22-68-1015-3
R30	, 0.9000Ω, (Note 2)	22-68-1015-4
R31	, 0.1000Ω, (Note 2)	22-68-1015-5
R32	, 180Ω, ¼W, 5%, C.C.	22-021819
R33	, 620Ω, ¼W, 5%, C.C.	22-026219
R35	, Variable, 500Ω, 10%	22-673501
R42, R58, R69	, Final Adjust, ¼W, C.C.	
R43, R44	, 10K, 1%, RN55C	22-341002
R45	, 47 MEG, ¼W, 5%, C.C.	22-024769
R52	, 3K, ¼W, 5%, C.C.	22-023029
R54	, 7.5 MEG, ¼W, 5%, C.C.	22-027559
R55	, 8.2K, ¼W, 10%, C.C.	22-028228
R56	, 180 MEG, ½W, 20%, C.C.	22-031877
R57, R92, R93	, 120K, ¼W, 5%, C.C.	22-021249
R60	, 100 Ω, 2W, 5%, C.C.	22-051019
R94	Resistor, 10K, ¼W, 5%, C.C.	22-021039
SW1	Switch, 3 Wafer	68-1000
SW2	Switch, 4 Wafer	68-1001
SW3	Switch	25-441001
T2	Transformer	68-1008
Z1	Int. Ckt., Oper. Amp.	24-421556
Z2	, Oper. Amp.	24-420301
Z3	, Oper. Amp.	24-400741
Z4	, Oper. Amp.	24-405558
Z5	, Oper. Amp.	24-400709
Z6	, 4030	24-L04030
Z7, Z8, Z9	, 4013	24-L04013
Z10	, Quad 2 Input NAND Gate	24-L04011
Z13	Int. Ckt., 4 Digit Disp. Ctr/Decoder	24-48-1010

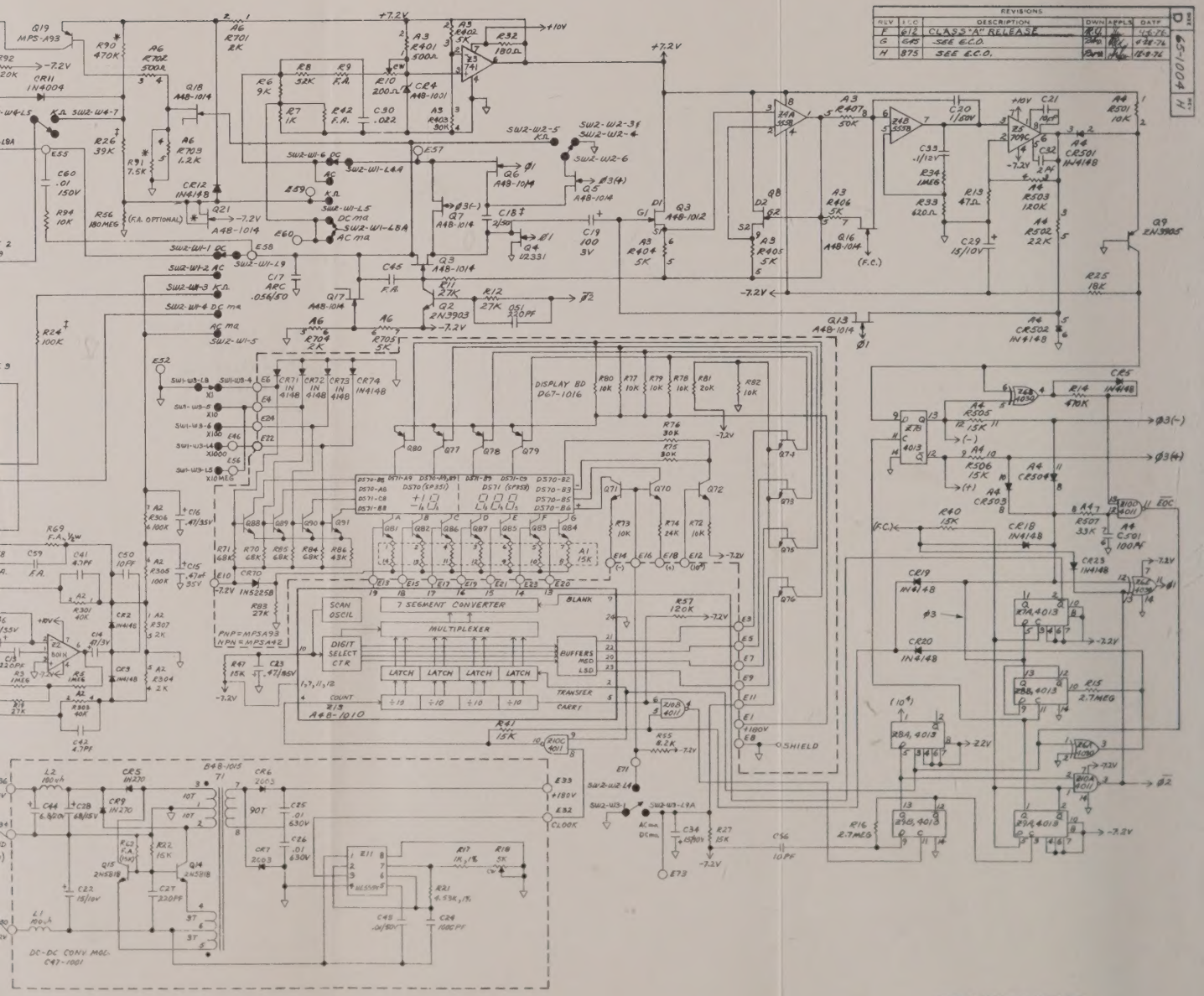
Note (1) Must be replaced as a set 22-48-1005
(2) Must be replaced as a set 22-48-1007

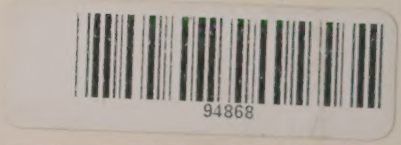


DISPLAY BOARD ASSY, D67-1016

REF. DESIG.	DESCRIPTION	PART NUMBER
A1	Resistor Network, 15K, 14 PIN	22-701000
CR70	Diode, IN5225B	24-120050
CR71-CR74	Diode, IN4148	24-110001
DS70	Display	25-210351
DS71	Display	25-210353
Q70-Q76, Q81-Q91	Transistor, MPSA42	24-230A42
Q77-Q80	Transistor, MPSA93	24-240A93
R70, R71, R84, R85	Resistor, 68K, ¼W, 5%, C.C.	22-026839
R72, 73. 82, 77-80	, 10K, ¼W, 5%, C.C.	22-021039
R74	, 24K, ¼W, 5%, C.C.	22-022439
R75, 76	, 30K, ¼W, 5%, C.C.	22-023039
R81	, 20K, ¼W, 5%, C.C.	22-022039
R83	, 27K, ¼W, 5%, C.C.	22-022739
R86	Resistor, 43K, ¼W, 5%, C.C.	22-024339


"THESE DRAWINGS AND SPECIFICATIONS ARE THE PROPERTY OF DATA PRECISION COMPANY AND SHALL NOT BE REPRODUCED OR COPIED OR USED AS THE BASIS FOR MANUFACTURE OR SALE OF APPARATUS WITHOUT EXPRESSLY WRITTEN AUTHORIZATION FROM DATA PRECISION COMPANY."
J1 (INPUT)
J2 (COMMON)
J3
J4
J5
AC IN
A1 A48-1009
R1 9/19K, 2W
RANGE 6
RANGE 5
RANGE 4
RANGE 3
RANGE 2
RANGE 1
R201 9MEG
R202 900K
R203 90K
R204 9K
R205 1K
C1 2-8 PF
C2 10-60PF
C3 10-60PF
C4 .018/50V
C5 150 PF
C6 1800PF
C11 .001/1KV
R53 100K
R28 90Ω
R29 9Ω
R30 .9Ω
R31 .1Ω
C48 15/10V
R45 10K, 1%
R35 500Ω
R44 10K, 1%
C7 10-60PF
C8 12 PF
C9, 10 PF
C10 .1/400V
R2 1MEG
C12 15/10V
R4 1K
R46 470K
R52 5.9K
R58 F.A.
R302 17.7K
R54 7.5 MEG
C47 1/12V
-12V
+17.2V
FS1 2A
FS2 1/10A
CR13 A48-1013
CR14 A48-1013
CR16 1N4148
CR1 1N4148
CR24 IN1204
CR25 IN1204
E60 2V
C53 330-F 35V
C40 68-F 16V
BAT.
R61 1/2 W 1.5K
R73 30Ω 1/2 W
C52 .01-F 1KV
SW3
Q22 MPS-A93
R93 120K


REVISIONS
REV | ECO | DESCRIPTION | DWN | APPR'D | DATE
F | 612 | CLASS "A" RELEASE | RCC | | 1-6-76
G | 645 | SEE E.C.O. | DMG | | 4-28-76
H | 875 | SEE E.C.O. | Bmk | | 12-8-76
D 65-1004 H
SCHEMATIC, 4 1/2 DIGIT DMM MODEL 1455
DISPLAY BD D67-1016
7 SEGMENT CONVERTER
MULTIPLEXER
SCAN OSCIL
DIGIT SELECT CTR
LATCH
BUFFERS
TRANSFER
CARRY
DC-DC CONV MOD. C47-1001
+7.2V
-7.2V
+10V
+180V
-22V
SHIELD
CLOCK



DATA PRECISION
Data Precision Corporation, Audubon Road, Wakefield, Ma. 01880

PRINTED IN THE U.S.A.
COPYRIGHT 1975
ALL RIGHTS RESERVED
62-5005-A